1.0 **SCOPE**

1.1 **General**

This specification covers the detail requirements for an electronic component.

2.0 **APPLICABLE DOCUMENTS**

The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, the issue in effect on date of latest revision of this specification shall apply.

2.1 **Atari Documents**

- C099901 Qualification, Reliability Requirements for Integrated Circuits and Discrete Semiconductors.
- C099902 Handling of Devices Susceptible to Static Discharge.

2.2 **ANSI Y32.14-1973 Logic Diagrams, Graphic Symbols for.**

3.0 **REQUIREMENTS**

3.1 **Electrical Requirements** — See Table I thru IV and Figures I and II.

3.1.1 Absolute Maximum Ratings in Free Air. Exceeding the "absolute maximum ratings," may result in failure or permanent damage to the part. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 **Logic Function**

Logic functions shall be as depicted in Figure (NA) as defined by American National Standards Institute Y32.14.

3.3 **Marking**

The part shall be marked with manufacturer's name or logo, type number, lot date code (on top), and Pin Number 1 identification.
3.4 Pin Assignment

Pin assignment shall be depicted in Figure I when related to package configuration in drawing.

3.5 Package Configuration

Package configuration shall conform to the requirements of drawing C099931 Dual in-line package.

3.6 Vendor Screen

Vendor screen shall conform to the Specification C099901. Burn-in circuit Figure III shall be used, 48 hrs. at 125 °C.

3.7 Package for Shipment

All parts shipped to this specification shall be packed in accordance with C099901 and C099902 to prevent physical damage, corrosion, static discharge and deterioration during shipment.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Vendor Qualification

Must meet the Atari Specification C099901, "Qualification, Reliability Requirements for Integrated Circuits and Discrete Semiconductors".
Functional Description

"Freddie RAM" is a custom LSI chip providing dynamic RAM control functions of the Atari "XL" home-computer products. It replaces a number of SSI and MSI TTL parts, including a custom delay line. Freddie RAM multiplexes 16-bit address bus into 8-bit row and 8-bit column address, and generates precisely timed row and column address strobes. Freddie RAM will be supplied in a 40-pin DIP with pin numbers shown below.

Pin Number  Name  Description (Apostrophe (?) denotes active-low)

DRAM Outputs

These multiplexed DRAM address bus outputs provide for direct connection to 64 K x 1 dynamic RAMs, selected from Intel 2164-20, Fujitsu MB 8264-20, Hitachi HM4864-3, NEC MPD 4164-2, Toshiba TMM 4164-4, Motorola MCM 6665A-20, or to 16 K x 4 dynamic RAMS, selected from Texas Instruments TMS 4416-20.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td>RA0</td>
<td>A0</td>
</tr>
<tr>
<td>31</td>
<td>RA1</td>
<td>A1</td>
</tr>
<tr>
<td>30</td>
<td>RA2</td>
<td>A2</td>
</tr>
<tr>
<td>29</td>
<td>RA3</td>
<td>A3</td>
</tr>
<tr>
<td>28</td>
<td>RA4</td>
<td>A4</td>
</tr>
<tr>
<td>27</td>
<td>RA5</td>
<td>A5</td>
</tr>
<tr>
<td>26</td>
<td>RA6</td>
<td>A6</td>
</tr>
<tr>
<td>25</td>
<td>RA7</td>
<td>A7</td>
</tr>
<tr>
<td>33</td>
<td>RAS'</td>
<td>DRAM Row address strobe output. A negative transition on this line indicates that RA0-RA7 contain a valid Row Address.</td>
</tr>
<tr>
<td>35</td>
<td>CAS'</td>
<td>DRAM column address strobe output. A negative transition on this line indicates that RA0-RA7 contain a valid Column Address.</td>
</tr>
<tr>
<td>36</td>
<td>16KCAS'</td>
<td>DRAM column address strobe output for first 16K only. Same as CAS' for addresses 0000-3FFF; always high for addresses 4000-FFFF. In Atari 600 with16K RAM, this line connects to RAM chips; CAS' connects to PBI.</td>
</tr>
<tr>
<td>34</td>
<td>Wrt'</td>
<td>WRITE' output to DRAM. This (transparent-) latched version of R/W' becomes stable shortly after R/W' and remains stable until after RAS' and CAS' have risen. See timing diagram.</td>
</tr>
</tbody>
</table>

* Note! These bits are ignored by 16Kx4 RAMs; they allow for possible 64Kx1 applications.
Memory Map Qualifier Inputs

| 3  | ExtSel’ | External Select input from parallel bus. Low forces CAS’ high (immediately, asynchronously) |
| 4  | CasInh’ | CAS-Inhibit input. Similar to ExtSel’ but latched. When CasInh’ is low at beginning of cycle, CAS’ is kept high for complete cycle. |

Miscellaneous Pins

| 40 | Vdd    | Power (+5 volts) |
| 20 | Gnd    | Ground (0 volts) |
| 8-19 | A0-A11 | Address bus input from CPU and ANIC |
| 21-24 | A12-A15 | Read/Write’ input from CPU |
| 38 | R/W’ | Reset input. A negative-going transition on this line sets the Wrt’ latch high (read mode), sets the CasInh’ latch to inhibit CAS’. This may take several Phi2 cycles. The chip then begins normal operation (without waiting for Reset’ to rise again). |

An internal inverter between pins 1 and 2 provides for direct connection to a 14.31818 MHz parallel–resonant, AT-cut crystal. Alternately, external clock square-wave may be input to pin 2.

| 1  | XTAL/CkOut | Output to crystal |
| 2  | XTAL/CkIn  | Input from crystal or Ext. clock input |
| 37 | OSC       | 3.579545 MHz output to GTIA |
| 5  | Phi2      | Clock “Phi2’’ input from 6502 CPU |
| 7  | OE’       | “Output Enable” output. |
| 6  | LE’       | “Latch Enable” output. |

Pins 6 and 7 provide control signals for use with an optional equivalent replacement for the FIA Port B register, as follows:

<table>
<thead>
<tr>
<th>OE’ LE’ Function</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>L L</td>
<td>Reset</td>
</tr>
<tr>
<td>L H</td>
<td>Read</td>
</tr>
<tr>
<td>H L</td>
<td>Write</td>
</tr>
<tr>
<td>H H</td>
<td>Hold</td>
</tr>
</tbody>
</table>
Required Operating Environment

Vdd  4.75  5.25  v  Power Supply Voltage
Tamb  0   70  C  Ambient temperature
VIH  3.5  5.0  V  Input High voltage (XTAL/ClkIn input only)
VIL  2.0  5.0  V  Input High voltage (all other Inputs)
VIL  -0.3  0.8  V  Input Low voltage
fOSC  14.31817 14.31819  MHz  Crystal Frequency
tCYC  559  560  ns  Phi2 Period
tLPhi2  250  320  ns  Phi2 low time
tRNV  145  145  ns  Phi2 falling to R/W' Valid
tABV  145  145  ns  Phi2 falling to Address Bus Valid
tRV  145  145  ns  Phi2 falling to Ref' Valid
tRWC  30  30  ns  Phi2 falling (again) to R/W' Change
tABC  30  30  ns  Phi2 falling (again) to Address Bus Change
tRC  30  30  ns  Phi2 falling (again) to Ref' Change
tCIS  250  250  ns  Setup; Phi2 falls to CI' valid
tCII  370  260  ns  CI' hold time after Phi2 falling
tESS  40  40  ns  ExtSel' setup after Phi2 falling
tESC  40  260  ns  Setup, ExtSel' to CAS' would fall
tESH  0  0  ns  ExtSel' hold time after CAS' rising

Operational Characteristics & Propagation Delays

Propagation delays are measured from when input crosses 1.5 v until output crosses 1.5 v.

Pd  0  500  mW  Power Dissipation
Cin  0  10  pF  Input Capacitance (all inputs)
Iin  -10  +10  uA  Input leakage current (0 < Vin < 5 v)
VOL  0  0.4  V  Output low voltage (Isink <= 1.6 mA)
VOH  2.4  5.0  V  Output high voltage (Isource <= 0.1 mA)
tr,tf  0  15  ns  Output rise, fall times (CL <= 80 pF)
trA  0  60  ns  Address bus to RAM Address pins
trAS  0  60  ns  Row Address Setup to RAS' falling
trAH  30  30  ns  Row Address Hold after RAS' falling
trSH  200  200  ns  RAS' low time
trF  135  135  ns  RAS' high time
trF  210  305  ns  Phi2 falling to RAS' Falling (read, write, or
refresh cycle)
tCR  10  100  ns  Phi2 falling to CAS' rising (from previous cycle)
tCRP  0  0  ns  CAS' rising (from previous cycle) to RAS' falling
tCAS  135  135  ns  CAS' low time
tCFN  35  35  ns  CAS' high time
trCD  80  80  ns  RAS' falling to CAS' falling
tCFR  300  370  ns  Phi2 falling to CAS' Falling (read cycle)
tCFW  425  425  ns  Phi2 falling to CAS' Falling (write cycle)
tASC  0  0  ns  Column Address Setup before CAS' falling
tCAH  80  80  ns  Column Address Hold after CAS' falling
tAR  135  135  ns  Column Address Hold after RAS' falling
tWRCS  0  0  ns  Wrt' setup before CAS' falls
twCH  80  80  ns  Wrt' hold after CAS' falls
trCH  0  0  ns  Wrt' hold after both RAS' and CAS' have risen
trNWR  50  50  ns  R/W' to Wrt' (transp. latch loading)
tLEF  240  360  ns  Phi2 falls to LE' falls, D301 Write
tLER  440  600  ns  Phi2 falls to LE' rises
toEF  240  450  ns  Phi2 falls to OE' falls, D301 read
tOER  570  660  ns  Phi2 falls to OE' rises
Note: tESS(max) and tCFR(min) are specified so that an external parallel device has adequate time, after ExtEn becomes valid, to assert ExtSel' at least tESC before CAS would fall.
FIGURE 1 - PIN DIAGRAM
FIGURE 3 - BURN-IN CIRCUIT

R = 5K - 10K

ANY CHANGES TO THIS CIRCUIT MUST BE APPROVED BY ATARI ENGINEERING