BUILD THIS DRAM TESTER FOR LESS THAN $60!

Take the guesswork out of determining whether your dynamic RAM chips are functioning properly and at the rated speed.

BUILD THE PHONE-COM

Use your telephones as a home intercom system.

BUILD A PULSE GENERATOR

Our handheld Pulse-Mate is a handy troubleshooting tool.

SWITCHING REGULATORS

The heart of switching power supplies.

PC-BASED TEST EQUIPMENT

Experimenting with the basic concepts.

64/256K

DT-90 DRAM TESTER

1 MEG   HI   5V   LO

CYCLE

100   2

80   150

STARTEK
INTERNATIONAL, INC.
FT. LAUDERDALE, FL

MARGIN

60   200

TEST   ACCESS TIME - ns

BUILD THIS

DRAM TESTER

Build a sophisticated DRAM tester with function, speed, and margin tests for under $60!

FRED HUFFT

IF YOU SERVICE OR EXPERIMENT WITH personal-computer hardware, you have probably handled a lot of memory circuits, commonly referred to as a "RAM" (random-access memory) or "DRAM" (dynamic RAM). When troubleshooting a PC memory problem, expanding RAM capacity, or upgrading the cycle speed of a memory bank, it can be very helpful to have a way of function testing and measuring the access time or speed of the DRAM IC's. Many intermittent memory failures have been traced to a slow DRAM in the memory bank. On the other hand, some DRAM's will far exceed their minimum access rating and can be speed tested and sorted for faster functions, saving the cost difference to the faster rated parts.

A number of small DRAM testers are available from about $150 to $1000, with the less-expensive models not having a lot of features. However, if you are interested in building a multi-featured unit that can function test, accurately speed test, and automatically cycle the tests under high-, low-, or normal-voltage margins, all for less than $60 (plus enclosure and AC adaptor), then check out this easy-to-assemble DRAM Tester.

Capabilities

The unit can test 64K × 1, 256K × 1, or 1MEG × 1 DRAM's, and can measure speed or access times from 60 to 200 nanoseconds (ns). There is a switch to select a "HI" and "LO" voltage-margin test and three LED indicators that show the current device-under-test (DUT) voltage. There's also a red/green LED that blinks green to show a test is running, displays a continuous green to show a test has run complete without an error, and will display a continuous red when a test is stopped by the detection of an error.

An 18-pin ZIF (zero insertion force) test socket is provided for

1-MEG DRAM's and a 16-pin ZIF test socket is used for the 64K and 256K DRAM's. A pushbutton TEST switch starts a test sequence, which runs about 10 to 14 seconds depending on the access speed. However, a CYCLE switch is provided to continuously recycle the selected test, if desired. When a 1-MEG DRAM is tested, a 0101 data pattern is written to all addresses in the DRAM, then each address is read back and compared for correct

data. An error stop will occur immediately during the read test if the data is not correct.

After the 0101 pattern test, a 1010 pattern is written to all locations, then read back and compared. The two-pattern test is automatically run twice; upon successful completion of the two-pattern double test, the tester stops and indicates a continuous green on the PASS/FAIL indicator.

A 256K DRAM receives the same test except that it's written

MAY 1991

33

to and read back 4 times during each test and a 64K DRAM receives the write/read test 16 times in each pattern. If the CYCLE switch is on, the test does not stop and will continue until an error is detected. If the MARGIN switch is on, the first two-pattern test cycle will be run at low-margin DUT operating voltage and the second cycle will automatically switch to high-margin DUT operating voltage. Should both the MARGIN and CYCLE switches be on, the tests will alternate from low- to high-margin voltage. All voltage and test signals are applied to both ZIF test sockets simultaneously, but only one DRAM can be tested at a time. DRAM's to be tested can safely be inserted or removed from the ZIF test sockets with the power on.

Dynamic RAM

DRAM's use multiplexed row and column address inputs; 64K DRAM's require only 7 address lines, 256K DRAM's require 9, and 1-MEG DRAM's require 10. Figure 1 shows a block diagram of a typical 256K × 1 DRAM, and Fig. 2 shows a typical 1-MEG DRAM. Address decoding and address latches are incorporated in the DRAM. To address the DRAM, row-address data is put on all address lines and clocked by the RAS (row address strobe) signal, then the column address data is put on the address lines and clocked by the CAS (column address strobe) signal. DRAM's have a READ/WRITE input pin, usually labeled $\overline{w}$, to control the type of operation; a DATA IN pin, D; and a DATA OUT pin, Q.

Data is held in dynamic RAM by the charge on internal capacitors. Since the charge degrades with time, the bits need to be "refreshed" or row addressed at approximately every 4 to 64 milliseconds. That is typically done by a RAS-only cycle through the row addresses—a normal read or write cycle will also accomplish the refresh. A 1-MEG DRAM may have a "test function" input (TF) at pin 4 that allows it to be tested 4 bits at a time; we do not use that function so the TF input is disabled by tying it to ground.

The timing of the address and strobe inputs is critical. A DRAM's "access time," or speed, is the time from RAS, which is the
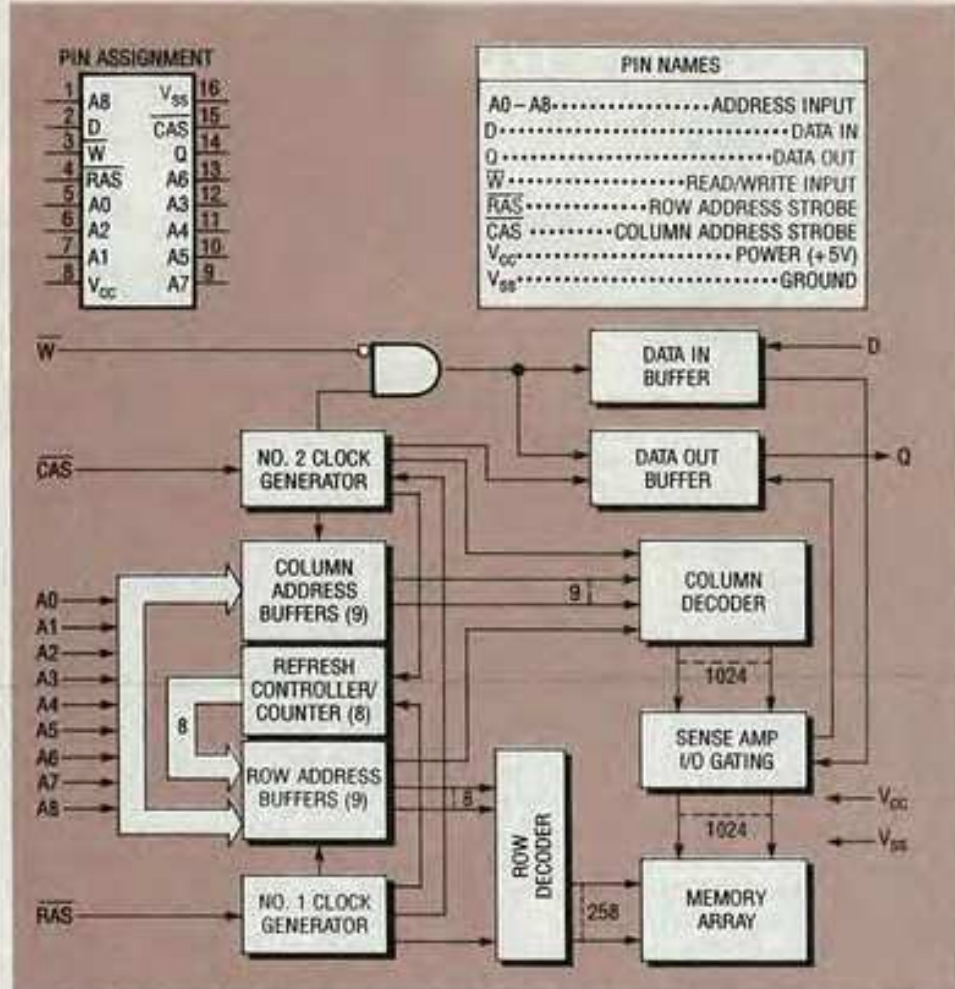

FIG. 1—256K DRAM PIN NAMES AND BLOCK DIAGRAM. DRAM's use multiplexed row and column address inputs; this 256K DRAM requires 9.

TABLE 1

	Parameter
t_{RC}	Random Read or Write Cycle Time
t_{RAC}	Access Time from $\overline{RAS}$
t_{CAC}	Access Time from $\overline{CAS}$
t_{OFF}	Output Buffer and Turn-Off Delay
t_{RP}	$\overline{RAS}$ Precharge Time
t_{RAS}	$\overline{RAS}$ Pulse Width
t_{CAS}	$\overline{CAS}$ Pulse Width
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time
t_{ASR}	Row Address Setup Time
t_{RAH}	Row Address Hold Time
t_{ASC}	Column Address Setup Time
t_{CAH}	Column Address Hold Time
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$
t_{RCS}	Read Command Setup Time

start of the addressing, to the time at which there is valid data at the output pin D. That is very basically how the DRAM works. Figure 3 shows a read-cycle timing chart for a 256K × 1 DRAM, and Table 1 explains what the timing symbols mean.

Circuit description

The DRAM tester uses two voltage-regulator IC's and only six logic IC's, thanks to the use of two PLD's (programmable logic devices) which replace about ten individual IC's. Refer to the block diagram in Fig. 4 and the sche-
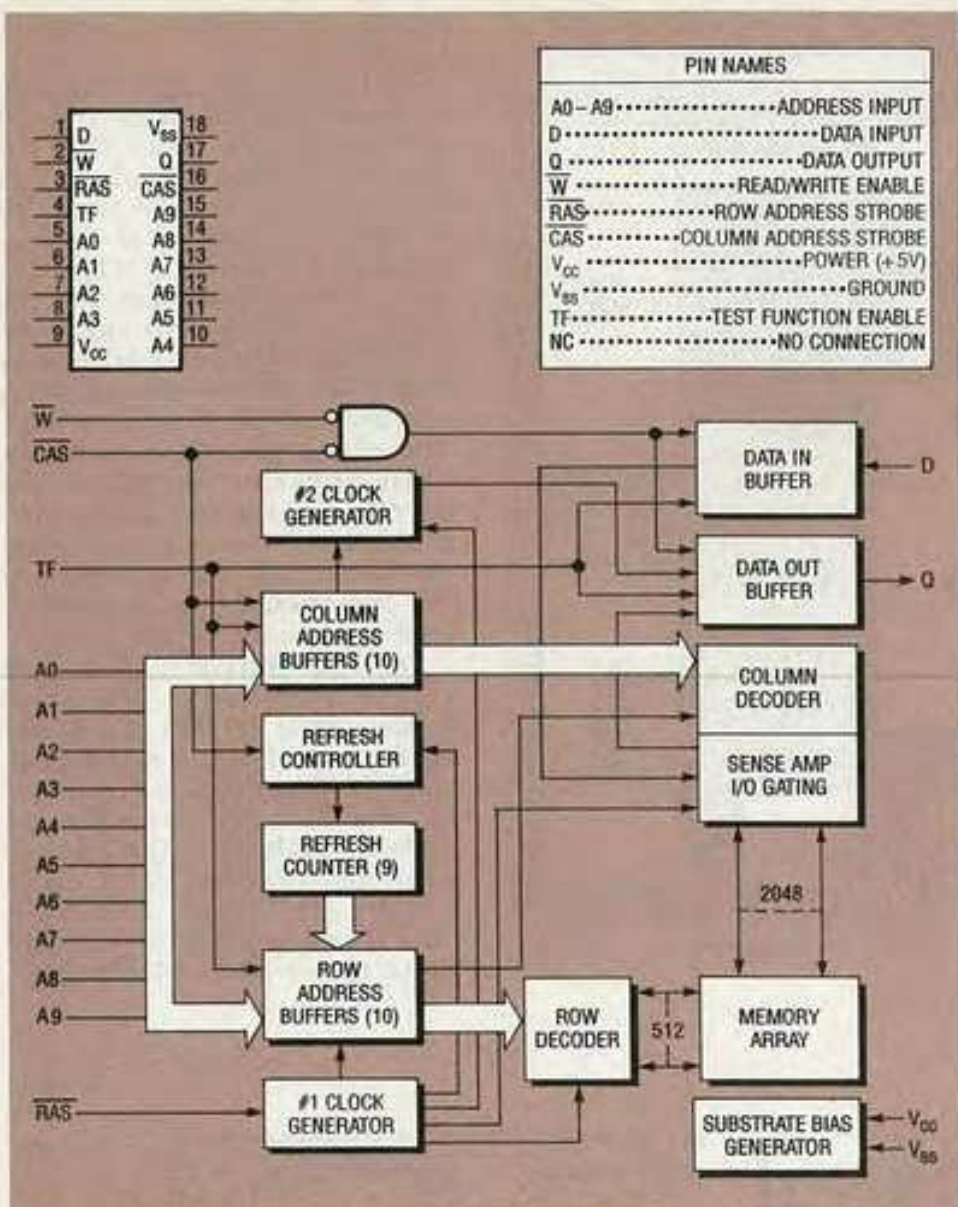
PIN NAMES	
A0 – A9	ADDRESS INPUT
D	DATA INPUT
Q	DATA OUTPUT
W̄	READ/WRITE ENABLE
R̄ĀS̄	ROW ADDRESS STROBE
C̄ĀS̄	COLUMN ADDRESS STROBE
V_{CC}	POWER (+ 5V)
V_{SS}	GROUND
TF	TEST FUNCTION ENABLE
NC	NO CONNECTION

FIG. 2—1 MEG DRAM PIN NAMES AND BLOCK DIAGRAM. Address decoding and address latches are incorporated in the DRAM.
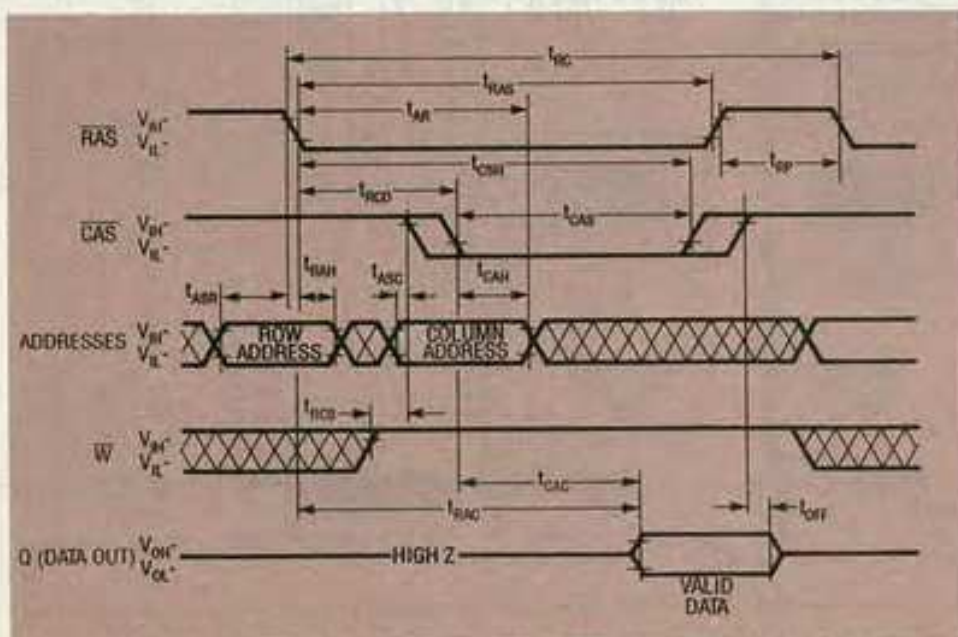

FIG. 3—DRAM READ CYCLE AND TIMING DIAGRAM for a 256K × 1 DRAM. Table 1 explains what the timing symbols mean.

matic in Fig. 5. An AC power adaptor supplies 9 volts DC at 150 mA to a full-wave bridge rectifier made up of D5–D8, which provide automatic input-polarity protection. The 5-volt regulator, IC7, supplies power to everything but the DUT (device under test). DUT power is supplied by IC8, an LM317LZ adjustable regulator which is controlled by logic in the PLD, IC5. For a normal test, IC8 outputs 5 volts to the DUT. Otherwise, 4.5 volts is supplied for the low-margin test and 5.6 volts for the high-margin test.

As mentioned before, IC5 and IC6 are TTL PAL devices; IC5 is an MMI/AMD PAL16L8B-2CN low-power, 25-ns device that contains the oscillator circuitry for our system clock. Components R15, R16, C12, and C5 are also part of the oscillator. The additional components R14, R5 (the access-time potentiometer), R19 (the calibration trimmer), and R17 (the dial-spread trimmer) form the speed-test circuit which varies the basic system clock.

The clock output at IC5 pin 15 is fed into IC6 pins 1 and 6. When the START TEST switch S1 is pressed, a START/RESET signal is generated through R7, C2, and R8 which resets IC2 and IC3 at pin 11; the signal is also applied as an input to IC6 pin 8. Logic in IC6 will gate an output clock signal, designated CLK1, at pin 14. That drives pin 10 of IC2 which is part of a 24-stage ripple-carry binary counter consisting of two 74HCT4040's (IC2 and IC3). As the clock increments the IC2/IC3 ripple counter, the Q0–Q7 and Q10–Q17 outputs drive IC1 and IC4, which are 74HCT257 quad 2-input multiplexers.

Multiplexers IC1 and IC4 each select four bits of data from two different sources under the control of a common select input at pin 1. Logic in IC6 generates the RAS signal which is input at pin 3 of IC5, present at pin 3 of test-socket ZIF1 and pin 4 of ZIF2, and is also the input select signal at pin 1 of IC1 and IC4. The outputs of IC1 drive address lines A0–A3 and the outputs of IC2 drive A4–A7 of the DUT at test sockets ZIF1 and ZIF2. A 256K DRAM requires an additional address line, A8, and a 1-MEG DRAM requires two additional address lines, A8 and A9. To gen-

erate the A8 and A9 address lines. Q8, Q9, Q18, and Q19 from IC2 and IC3 are logic inputs to IC6 which generates the A8 output at pin 19 and the A9 output at pin 12.

Both PAL's (the 16R4 and the 16L8) are rated at 25-ns internal gate propagation delay. That delay is an integral part of the system timing, and is used to determine the timing of the low CAS signal at pin 12 of IC5 about 40 ns after RAS goes low. The CAS signal is applied to the DUT which gates the column-address data after the row-address data has been gated. At the intersection of the row address and column address, we have the selected bit location. Output Q20 (IC3 pin 12) from the 24-stage ripple counter will determine if the operation will be a write or read cycle in the DRAM.

From the start of the test, Q20 applies a low to the DUT READ/WRITE inputs at ZIF1 pin 2 and ZIF2 pin 3. The low signal puts the DRAM in the write mode for the first half of the test, where we cycle through all of the address locations. Note that, as the ripple counter gets to Q20, we have cycled through all address locations in a 1-MEG DRAM once,
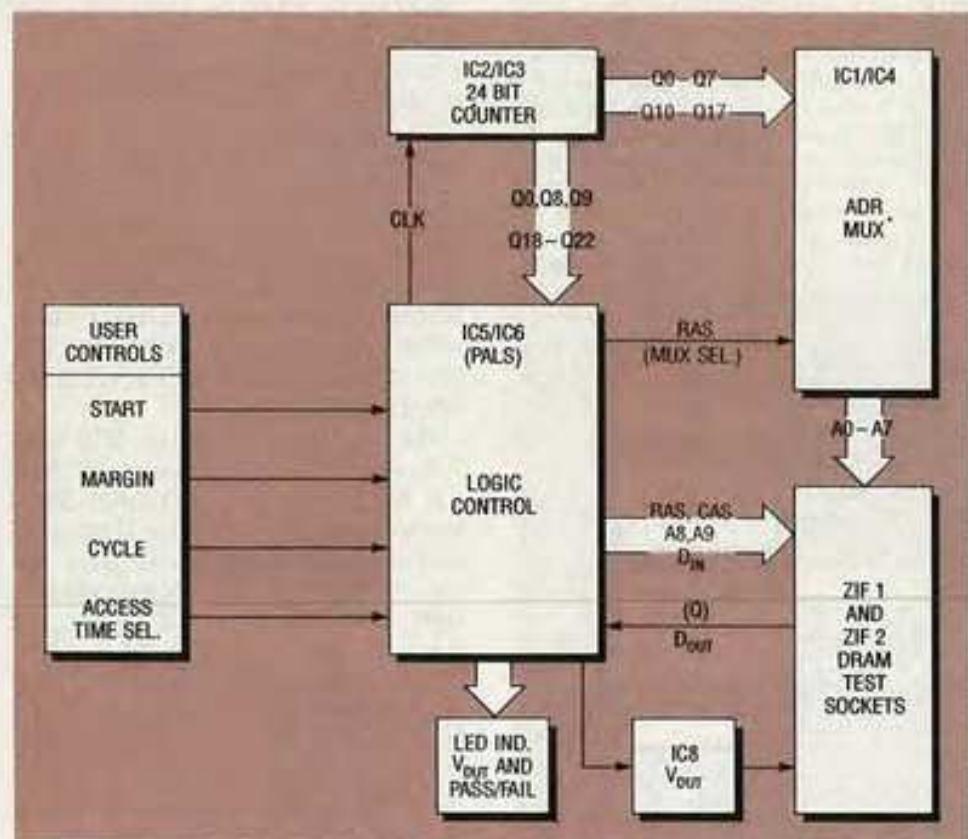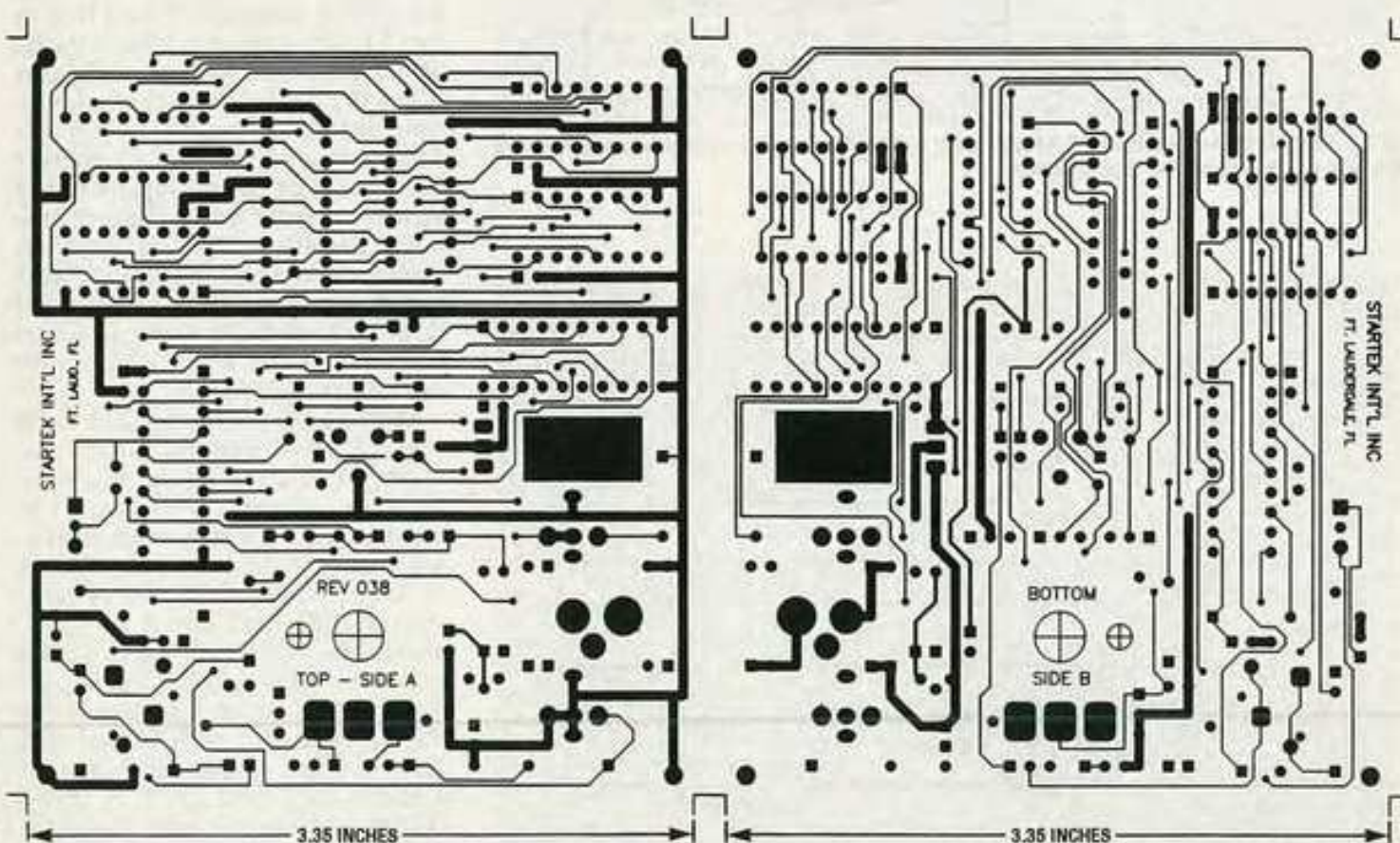

FIG. 4—DRAM TESTER BLOCK DIAGRAM. The DRAM tester uses only six logic IC's, thanks to the use of two PLD's.

TOP, OR COMPONENT SIDE of the DRAM tester PC board. Parts are actually mounted on both sides of the board.
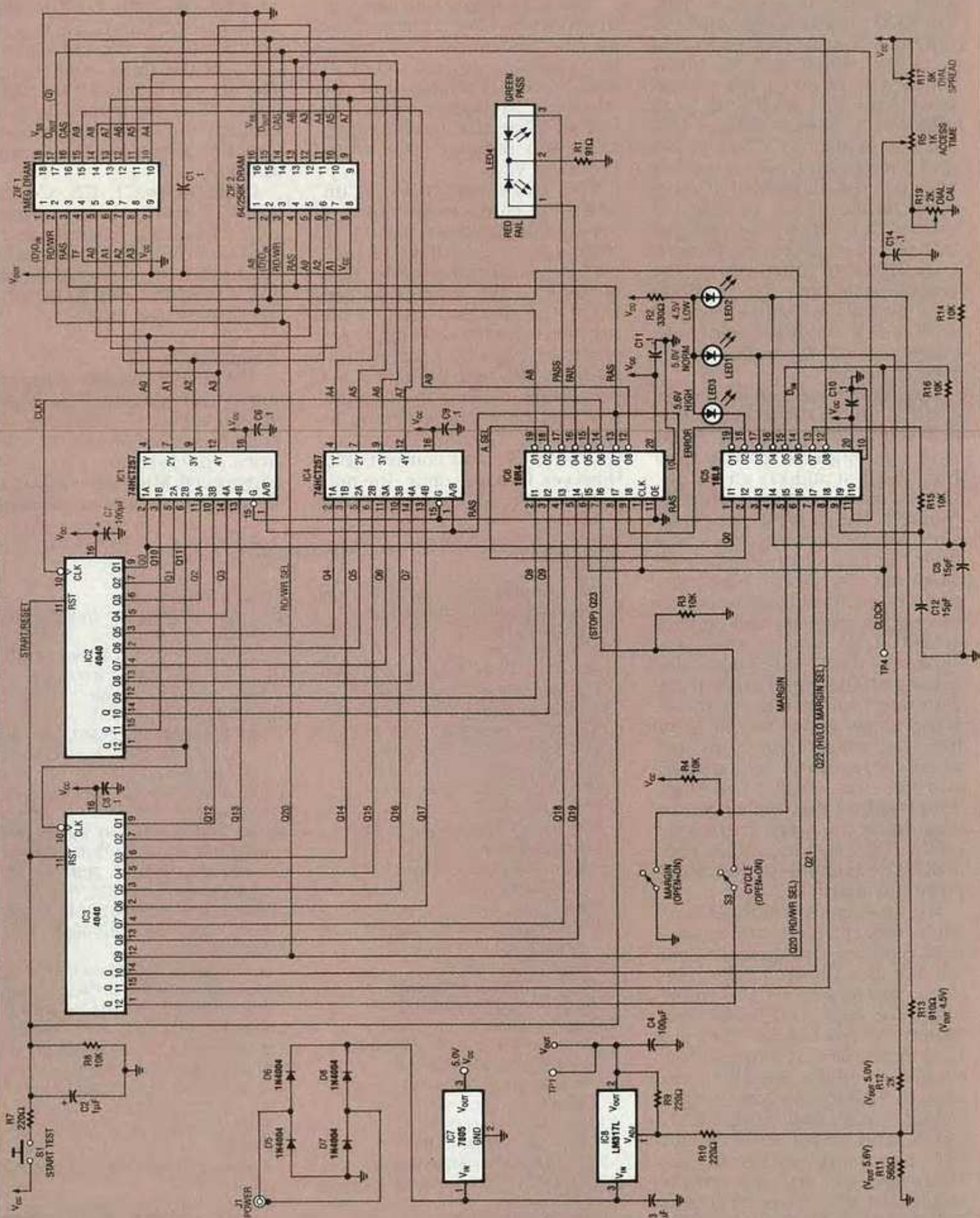
BOTTOM, OR SOLDER SIDE of the board.

FIG. 5—DRAM TESTER SCHEMATIC. The 5-volt regulator, IC7, supplies power to everything but the DUT, which is powered from IC8, an LM317LZ adjustable regulator. IC8 normally outputs 5 volts to the DUT; 4.5 volts is supplied for the low-margin test and 5.6 volts for the high-margin test.

four times in a 256K DRAM, and sixteen times in a 64K DRAM. The Q20 output is also input to pin 6 of IC5, which will generate a D_{IN} signal, which will determine the data bit (high = 1, low = 0) applied to the DUT at ZIF1 pin 1 and ZIF2 pin 2. Signals Q0 and Q21 are also applied to IC5 at pins 1 and 7 respectively; Q0 is used to alternate the bit pattern at every other location as it is triggered every cycle or clock time, and Q21 is used to change the pattern from 010101 to 101010 during the second write cycle. Every DRAM location will have both a 1 and a 0 written to it and read back 1 to 16 times per test, depending on the type of DRAM.

During the read cycle, the access time of the DRAM is the time between the RAS and D_{OUT} (valid data out) signals, or the time from the first address strobe until valid data is at the Q output of the DUT. The Q output is a three-state signal that switches to a high-impedance mid-logic level when the CAS signal goes inactive. As each address is cycled through during the read portion of the test, the data bit read out is applied to pin 11 of IC5 and compared with the expected bit. If the data does not match, an ERROR signal is generated at pin 19 of IC5 that goes to pin 9 of IC6 where the FAIL output will go high and the CLK1 output will stop. That will halt the ripple counter and make pass/fail indicator LED4 light a continuous red. (LED4 should have been blinking green during the test.)

The MARGIN switch S2 is "on" when the contacts are open— that removes the ground from pin 5 of IC5, allowing pull-up resistor R4 to switch the input high. The logic in IC5 will then switch the low output from pin 17, which selected a normal DUT operating voltage of 5.0V, to pin 16, which selects a low-margin voltage of 4.5V. Indicators LED1, LED2, and LED3 show which DUT operating voltage is currently selected, and will remain illuminated after an error stop to indicate what operating voltage was selected at the time of failure. The Q22 input at pin 8 of IC5 will switch the low-margin test to high, and select the pin-18 output of IC5, which lights LED3 to indicate a high-margin operating

voltage of 5.6V.

The IC5 outputs that select the appropriate LED indicator also directly control the DUT voltage by applying a ground to R12 via pin 17, R13 via pin 16, or neither when pin 18 (high margin) is selected. That affects the adjustment pin regulator IC8 which produces V_{DUT}.

The CYCLE switch S3 is "on" when the contacts are open, allowing the pull-down resistor R3 to hold pin 7 of IC6 low. The highest bit in our ripple counter, Q23, is the STOP bit. When Q23 goes high, the two-pattern test has run twice. Switch S3 simply prevents the high Q23 output from reaching the logic input of IC6. If you prefer cycling the two-pattern test once and stopping instead of twice, simply disconnect Q23 from S3 and connect Q22. However, if that is done, the margin test would have to be run

with the CYCLE switch also "on" so that the high-margin test is run. With actual usage, it is convenient to use the CYCLE switch most of the time. Just increase the access time until the DRAM fails, then decrease the speed slightly and restart the test to quickly determine the speed of the part.

Capacitors C1, C3, C6, and C8–C11 are for power bypass, and R1 is used to limit the current flow through LED4. Resistor R2 limits the current through LED1, LED2, and LED3, which are discrete red LED's.

Using PAL's

The programmable array logic device, known as a PAL, was invented about 15 years ago at a company called Monolithic Memories, which is now part of AMD (Advanced Micro Devices). The PAL provides a way of combining

PARTS LIST

All resistors are ¼-watt, 5%, unless otherwise noted.
R1—91 ohms
R2—330 ohms
R3, R4, R8, R14–R16—10,000 ohms
R5—1000 ohms, linear taper potentiometer
R6, R18—not used
R7, R9, R10—220 ohms, 1%
R11—560 ohms
R12—2000 ohms, 1%
R13—910 ohms
R17—5000 ohms, 4-turn trimmer potentiometer
R19—2000 ohms, trimmer potentiometer
Capacitors
C1, C3, C6, C8–C11, C14—0.1 μF, monolithic
C2—1 μF, tantalum
C4, C7—100 μF, electrolytic
C5, C12—15 pF, monolithic
Semiconductors
IC1, IC4—74HCT257 quad 2-channel three-state multiplexer
IC2, IC3—74HCT4040 12-stage binary counter
IC5—AMD 16L8B-2 PAL
IC6—AMD 16R4A-4 PAL
IC7—LM7805 5-volt regulator
IC8—LM317LZ low-power adjustable regulator
D1–D4—not used
D5–D8—1N4004 1-amp rectifier diode
LED1–LED3—red light-emitting diode, ⅛-inch diameter
LED4—red/green 3-lead common-cathode LED module

Other components
S1—normally-open pushbutton switch
S2, S3—SPDT sub-mini slide switch
J1—2.1 mm DC power input jack
ZIF1—18-pin ZIF socket
ZIF2—16-pin ZIF socket
Miscellaneous: PC board, four 16-pin IC sockets, two 20-pin IC sockets, knob for R5, cabinet, 120-VAC-to-9-VDC 300-mA wall adapter, solder, etc.
Note: The following items are available from Startek International Inc., 398 NE 38th St., Ft. Lauderdale, FL 33334. For information call (305) 561-2211, for orders call (800) 638-8050, FAX (305) 561-9133.
● **Complete DRAM tester kit including programed PAL's (does not include cabinet and AC adaptor), KIT #DT-90K—$59.95.**
● **Complete DRAM-tester kit including programed PAL's, cabinet, and AC adaptor, KIT #DT-90CK—$89.95.**
● **PC board only, #DT-90PCB—$18.00.**
● **Programed PAL's—$7.50 each.**
● **A factory assembled, calibrated, and tested DRAM tester—$119.00.**
Add 5% shipping/handling charge ($4.00 minimum, $10.00 maximum.) Florida residents must add sales tax. VISA, MC and COD-CASH orders accepted.

a number of discrete logic IC's in a single custom-programed IC. The PAL device has a programmable AND array followed by a fixed OR array. In the DRAM-tester circuit we use two very common PAL's, a 16L8 and a 16R4. Both are low-power devices, and relatively inexpensive.

The use of PAL's results in reduced parts count and power consumption, a smaller PC board, faster logic, increased reliability, and, usually, overall reduced cost. A reduced parts count means less-complex PC boards are required, and circuit changes can frequently be made in the PAL program without affecting the PC board. On the down side, designing with PAL's does require support tools consisting of design software and a device programmer. (Those items are needed by the circuit designer; the builder does not require those items, as programed PAL's are available from the source listed in the parts list.) The PAL design software provides the link between high-level logic expressions and the low-level programming details which the device programmer uses.

In our circuit, IC5 (a 16L8 PAL) has 10 dedicated inputs, 2 dedicated outputs, and 6 combinatorial input/output pins. IC6 is a 16R4 PAL which has a 4-bit register, a clock register input, 8 dedicated inputs, 4 registered outputs with an output-enable pin, and 4 combinatorial input/output pins. Both are 20-pin DIP TTL devices, which are one-time programmable by opening fuse links (with an appropriate device programmer) to configure the AND and OR gates within the device. The PAL devices implement the Boolean logic transfer function, the sum of the products. The AND array creates custom product terms, while the OR array sums selected terms at the outputs of the device.

Figure 6 shows the pinouts for the 16L8 and 16R4 PAL's with the input/output signals and logic equations used to generate each output. Figure 7 shows the logic diagram for the 16L8 and Fig. 8 shows the 16R4. A PAL is manufactured with all "fuses," or connections intact. The undesired fuses are blown open by the programmer, leaving only the desired logic connections.
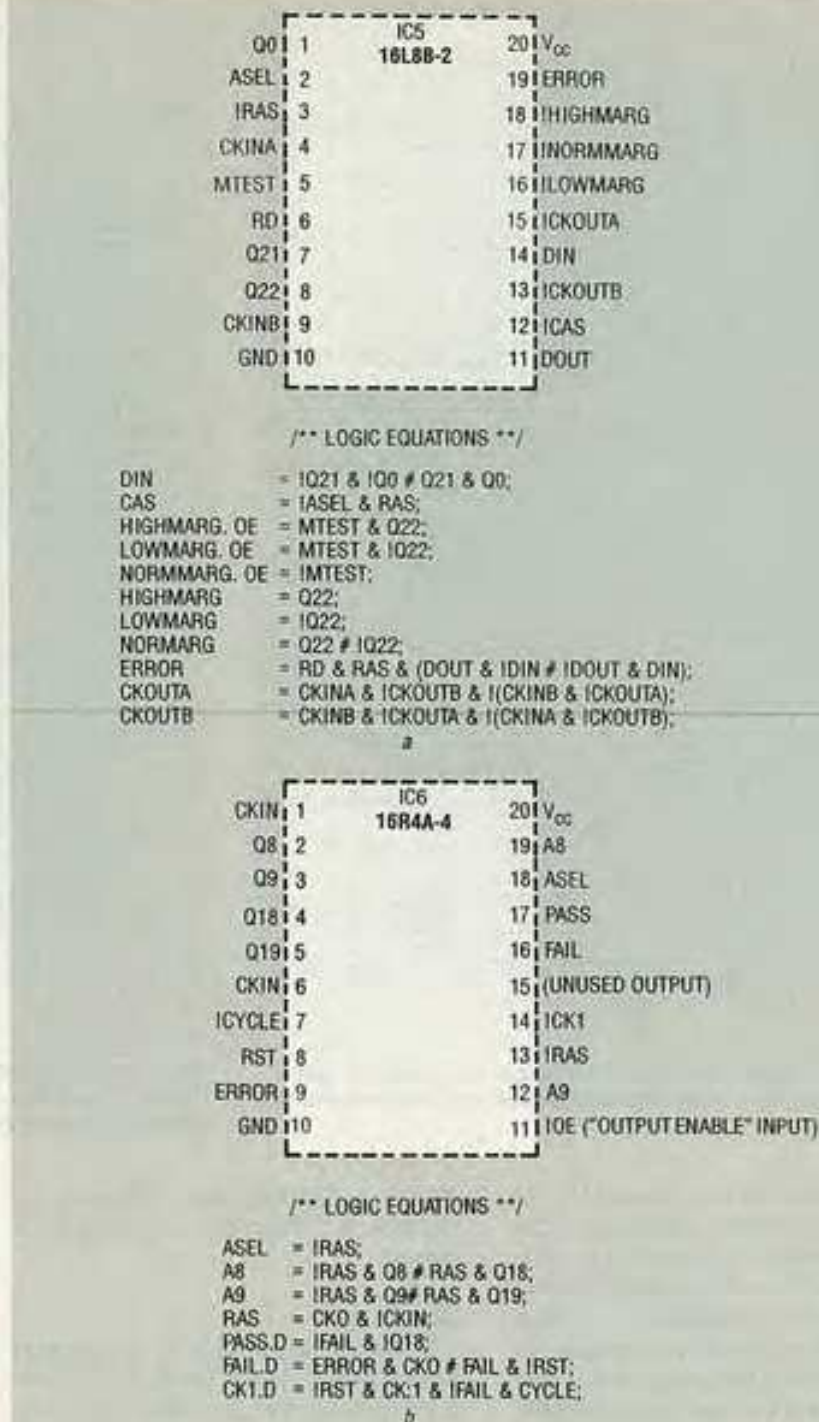
Assembly

The DRAM tester is easy to assemble. Parts are installed on both sides of a double-sided plated-through PC board measuring 3.35×3.8 inches. Programed PAL's, as well as the other parts including the PC board, are available from the source listed in the parts list. The professional-looking case you see is also available at extra cost. Parts assembly order is not critical, however, it's recommended that you install all resistors first, then di-

odes, IC sockets (not including the ZIF sockets), IC7 and IC8, and then the capacitors. Follow Fig. 9 for correct placement of parts.

Next install power-jack J1, and switches S1, S2 and S3. Be sure S2 and S3 are straight so that they will properly fit in the cabinet openings. Next install potentiometers R5, R17, and R19; R5 mounts under the PC board with the pins bent upward to fit the connection holes from under the PC board.

The two-color (red/green) LED (LED4) is probably the most diffi-

FIG. 6—PAL PINOUTS AND LOGIC EQUATIONS. 6-*a* shows the pinouts for the 16L8 and 6-*b* shows the 16R4. The logic equations are used to generate the outputs.

```
          ┌────────────┐
   Q0| 1  │    IC5     │ 20|Vcc
 ASEL| 2  │  16L8B-2   │ 19|ERROR
 IRAS| 3  │            │ 18|!HIGHMARG
CKINA| 4  │            │ 17|!NORMMARG
MTEST| 5  │            │ 16|!LOWMARG
   RD| 6  │            │ 15|CKOUTA
  Q21| 7  │            │ 14|DIN
  Q22| 8  │            │ 13|CKOUTB
CKINB| 9  │            │ 12|CAS
  GND|10  │            │ 11|DOUT
          └────────────┘
```

/** LOGIC EQUATIONS **/

```
DIN           = !Q21 & !Q0 # Q21 & Q0;
CAS           = !ASEL & RAS;
HIGHMARG.OE   = MTEST & Q22;
LOWMARG.OE    = MTEST & !Q22;
NORMMARG.OE   = !MTEST;
HIGHMARG      = Q22;
LOWMARG       = !Q22;
NORMMARG      = Q22 # !Q22;
ERROR         = RD & RAS & (DOUT & !DIN # !DOUT & DIN);
CKOUTA        = CKINA & !CKOUTB & !(CKINB & !CKOUTA);
CKOUTB        = CKINB & !CKOUTA & !(CKINA & !CKOUTB);
```

a

```
          ┌────────────┐
  CKIN| 1  │    IC6     │ 20|Vcc
    Q8| 2  │  16R4A-4   │ 19|A8
    Q9| 3  │            │ 18|ASEL
   Q18| 4  │            │ 17|PASS
   Q19| 5  │            │ 16|FAIL
  CKIN| 6  │            │ 15|(UNUSED OUTPUT)
!CYCLE| 7  │            │ 14|CK1
   RST| 8  │            │ 13|!RAS
 ERROR| 9  │            │ 12|A9
   GND|10  │            │ 11|!OE ("OUTPUT ENABLE" INPUT)
          └────────────┘
```

/** LOGIC EQUATIONS **/

```
ASEL    = !RAS;
A8      = !RAS & Q8 # RAS & Q18;
A9      = !RAS & Q9 # RAS & Q19;
RAS     = CKO & !CKIN;
PASS.D  = !FAIL & !Q18;
FAIL.D  = ERROR & CKO # FAIL & !RST;
CK1.D   = !RST & CK1 & !FAIL & CYCLE;
```
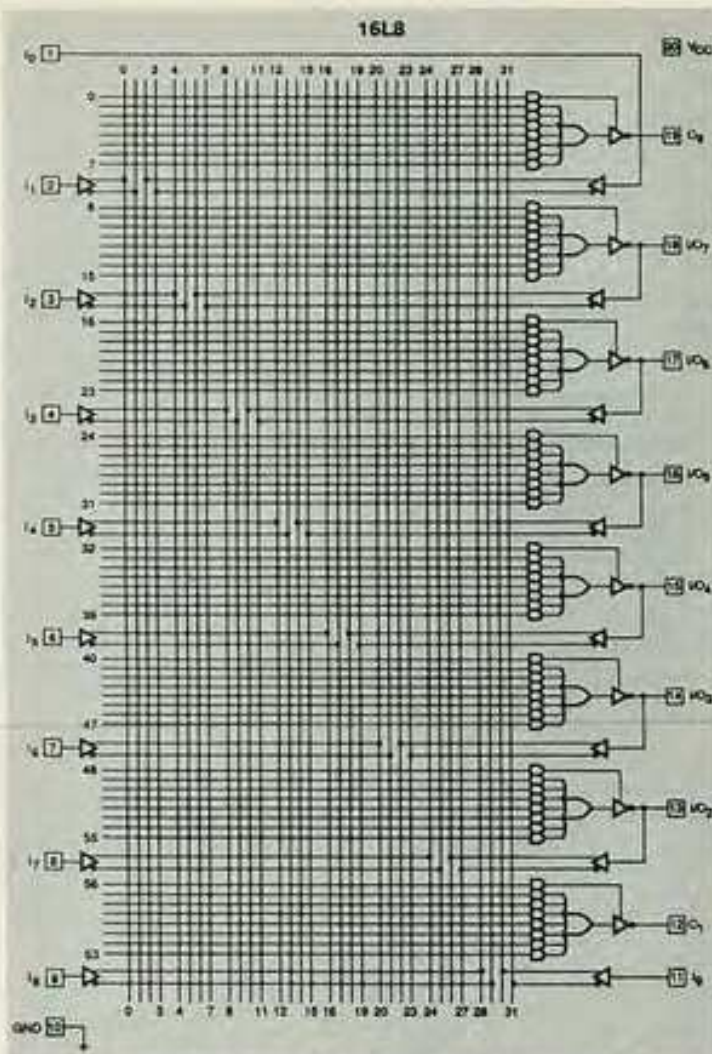
b

FIG. 7—16L8 LOGIC DIAGRAM. This 20-pin DIP device is one-time programmable by configuring the AND and OR gates within the device.
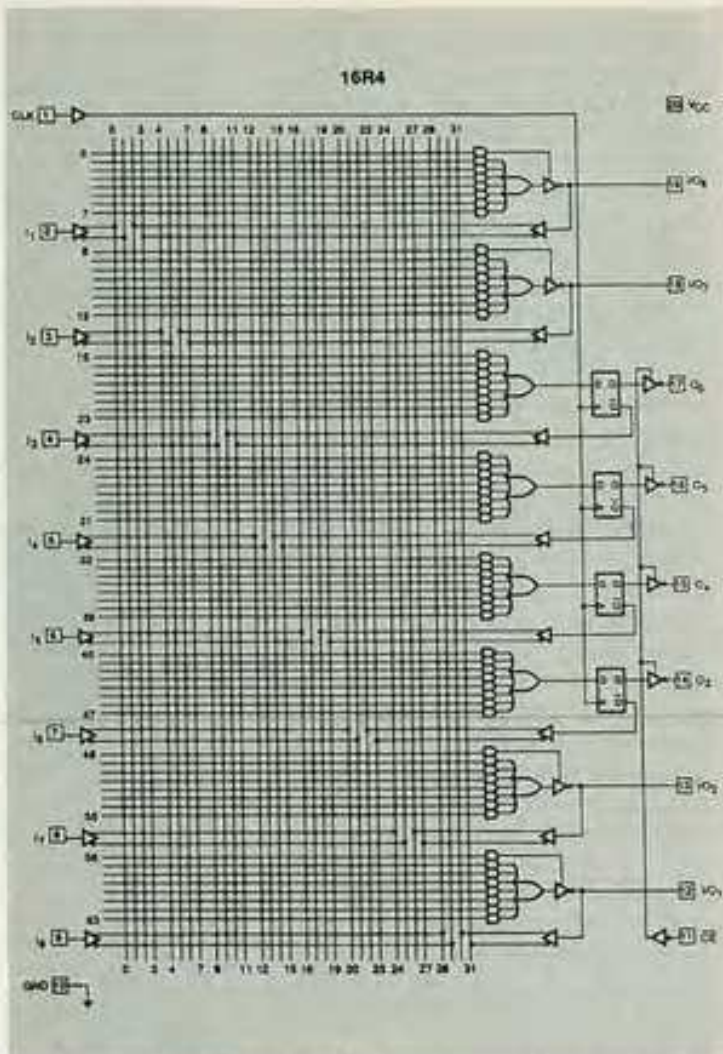

FIG. 8—16R4 LOGIC DIAGRAM. A PAL is manufactured with all "fuses" intact. The undesired fuses are blown open by the programmer, leaving only the desired logic connections.

cult component to install. Be sure to observe polarity; the slightly shorter lead is the red-LED anode (+), the center lead is the common cathode (−), and the remaining lead is the green-LED anode. Holding the LED with the shorter lead on your left, bend the center lead at a 90-degree angle, snug against the component body, toward yourself, and likewise bend the other two leads in the opposite direction, spreading them slightly. Align LED4 over the proper PC-board location and bend the three leads down to fit the holes. Check for proper alignment with the cabinet before soldering.

Install LED1, LED2, and LED3. Note that the flat side of the LED's is the cathode. Allow the LED's to stand about ⁷/₃₂-inch above the PC board. Install the two ZIF sockets and insert IC1–IC6 into the appropriate sockets. Recheck all component connections and polarities. If you are satisfied that everything looks correct, you're ready to continue. Figure 10 shows a photo of a completed board.

Checkout

Set R17 and R19 to midpoint adjustment. With no device in either test socket, connect a 9-volt DC power supply, rated at 200 mA or more (the actual current draw will be about 150 mA), to J1. (The polarity does not matter as we have a diode-bridge power input.) A continuous red should be displayed on LED4, the pass/fail indicator.

Using a DC voltmeter, make the following measurements. (Note that a ground pad is located in each corner of the PC board.) These voltages should be within ± 0.1 volt:

● IC7 pin 3 (V_{CC}) should be 5.0V.
● With the MARGIN switch (S2) off (slider to right), measure V_{DUT} at TP1. It should be 5.0V.
● With the MARGIN switch on, the low-margin DUT voltage indicator should be on and TP1 should measure 4.5V.

● Place a DRAM IC in the appropriate ZIF test socket, turn the access-time potentiometer (R5) fully clockwise and press test-switch S1. If the device under test is good and the tester is working properly, LED4 will blink green and, if the MARGIN switch is on, the tester should alternate between high- and low-margin voltages. If you do not get a correct indication, try a power off and on reset. Turn on the CYCLE switch (slider to the left) and the tester should repeat the test without having to press the TEST button.
● When the high-margin voltage indicator LED3 is on, the voltage at TP1 should be 5.6V.

If all of the above voltages check out properly, only the "speed" or access-time calibration remains. If you have access to a 100-MHz oscilloscope, look at TP4 with no IC in either test socket. That is the master clock and it should run continuously. Allow the unit

ter the appropriate values into the Zero Offset and Low Factor fields. Also, change the μF limit to 1. Save the new data and re-execute CAP. Press M to measure. Disregard the value, but note the count, and multiply it by 10 to obtain the high factor. For example, if the count is 1234, the high factor is 12340. Execute CAPFAX one more time to enter the high factor and change the μF limit back to 10000. Save the revised data.

Use

Using the PC-based capacitance meter is straightforward. With your PC on and the meter connected to the printer port, apply power to the meter. At the DOS prompt, type CAP and press Enter. Insert the capacitor to be measured, and press M. The value appears in the middle of the screen, and the bottom indicates the range (pF, μF low, μF high), along with the timer count. To end the program, press E.

The μF limit and pF limit factors are used to determine how to format the measured value. If you measure a capacitor that displays 0.00 μF, but has a count greater than 0, you are in a "no-man's land" between the two limits. Execute CAPFAX and increase the pF limit factor. Doing so increases the pF formatting range and allows the measured value to be displayed properly.

Remember that if you vary the meter circuit or your PC, you should recalibrate the software to maintain accuracy.

Next Time

In the near future we'll incorporate the capacitance-measurement circuitry into a combination instrument that measures resistance, capacitance, and voltage. The device allows you to measure resistors, capacitors, diodes, and transistors. Because it is computer controlled, it can be the heart of an automated inspection system for your shop or business. You can save a lot of troubleshooting time by ensuring that the ICs you plan to use in a project function properly before you use them. The last project in this series is an IC tester that allows you to verify operation of most 14- and 16-pin TTL and CMOS IC's.   R-E

to operate a few minutes for maximum stability, set R5 at 100 ns on the dial, and adjust R19 for a low clock pulse of 200 ns. Measure the pulse at the 1.0-volt DC level. Next turn R5 fully counter-clockwise; the low clock pulse should be 150 ns. Turn R5 fully clockwise; the low clock pulse should be 300 ns—if not, adjust R17 for the proper "dial spread."
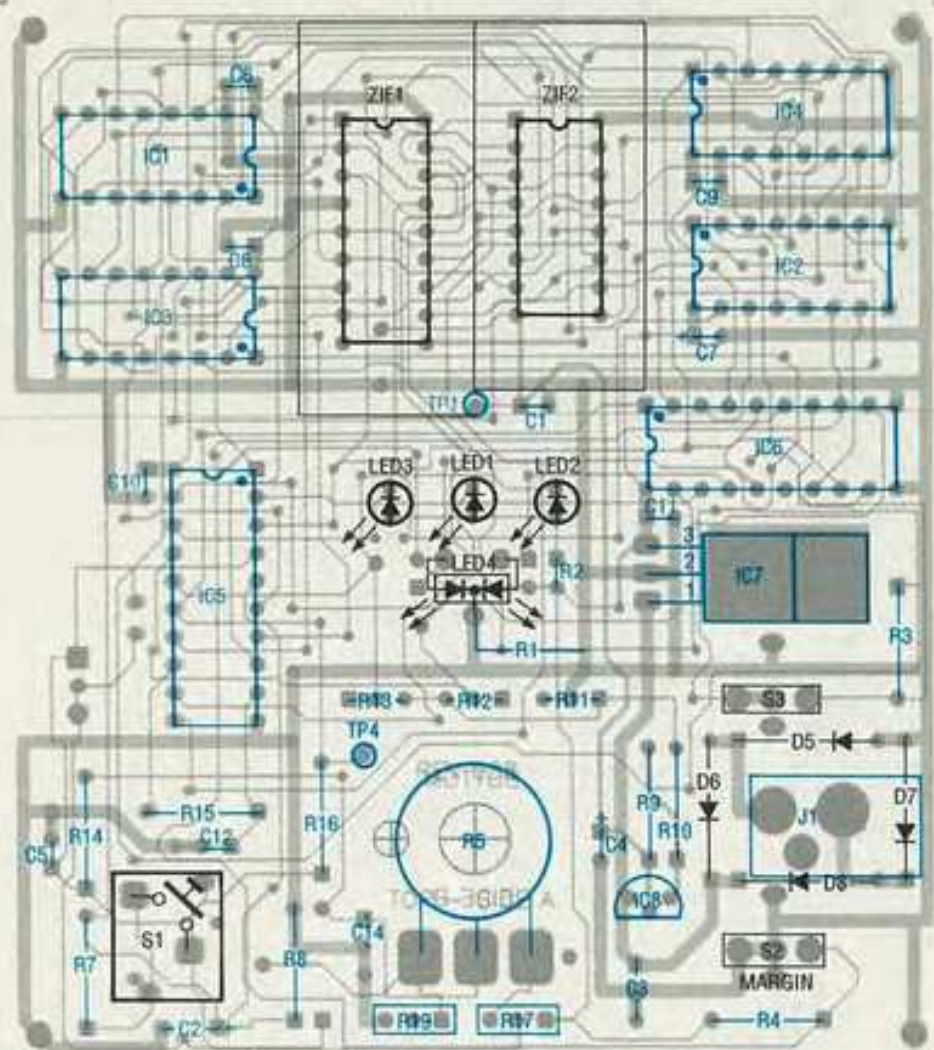

FIG. 9—PARTS-PLACEMENT DIAGRAM. The parts shown in color are installed on the "bottom," or solder side of the board—that is, the side opposite that with the ZIF sockets.
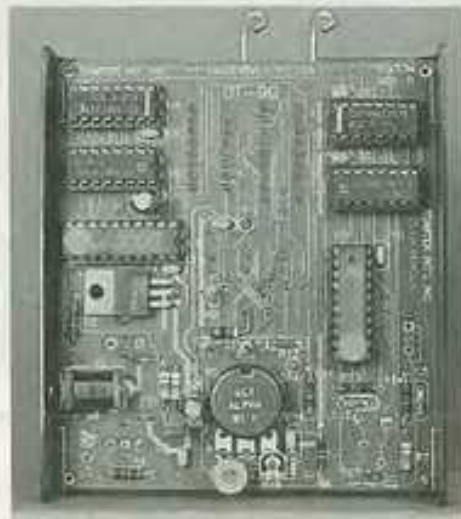

FIG. 10—THE FINISHED BOARD is neat and compact—and, of course, quite useful.

The R17 and R19 adjustments will interact somewhat, so adjust by small increments, and again calibrate R19 at the 100-ns dial setting with R5 after each change to R17. This adjustment should be easy; both potentiometers should end up somewhere near midrange.

If you do not have a scope immediately available to calibrate the access-time control, set R17 and R19 to midrange, which should be near calibration, and use the speed test for a relative indication; the function and voltage margin tests should work fine. All you have to do now is install the unit in an appropriate case and put it to good use.   R-E