MULTI-STANDARD PRINTER BUFFER

Leycester Whewell's micro is quick off the mark thanks to this 256K printer buffer with Centronics and RS232 interfaces.

Almost irritating feature of many printers is their data acceptance rate. Many have sufficient capacity to hold only a single line of text, although some can store 2K, 4K or 8K of data. So, when listing a program or document of any reasonable size, the computer is effectively slowed down to the speed of the printer.

A printer buffer appears as a very fast printer to the computer, storing its output so that the operator can get on with the next task without an enforced coffee break. Meanwhile, the buffer outputs data to the printer at its normal speed.

Features

Although the idea of a printer buffer is not a new one (and designs have appeared in ETI before) this device has an ample memory capacity of either 64K or 256K — approximately 20 or 80 pages of A4 text respectively.

The buffer also allows parallel-parallel, serial-parallel, parallel-serial and serial-serial data transfers with a serial data rate of either 1200 or 9600 baud. This should accommodate just about any combination of printer and micro.

The unit is driven by an 8-bit microprocessor, the 6803 (see Fig. 1). This is a 6800 with the added features of 128 bytes of zero page RAM, a timer, a serial communications interface, parallel I/O and some additional instructions.

Since the 6803 has only one serial interface, with I/O handshaking, one half is used to receive data and the other to transmit data. This combination prevents the use of XON and XOFF handshaking as an alternative to RTS and CTS. The same clock source drives both the receiver and transmitter, so serial-serial transfers must be at the same baud rate.

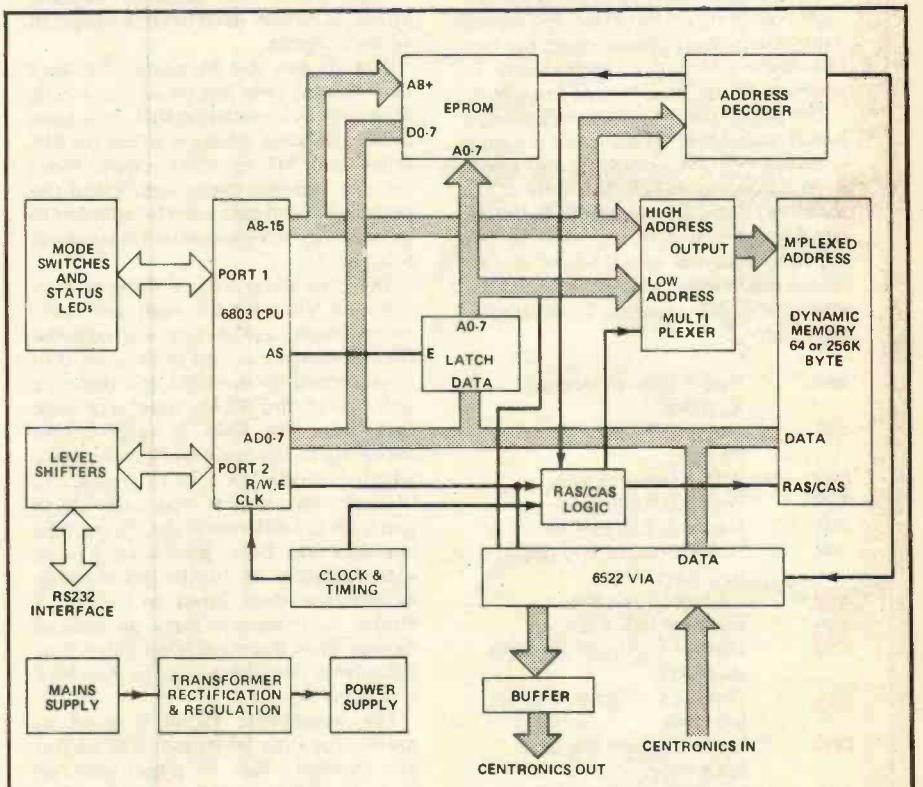


Fig. 1 Block digram of the printer buffer.

A rotary switch selects the desired transfer combination with an eighth position reserved for a self test mode. This checks the memory and the parallel and serial interfaces. The status of each is indicated by flashing the LEDs on the front of the unit.

A PAUSE switch halts the output to the printer although data is still accepted from the host micro and the RESET switch resets the entire unit, clears any data present and allows a new operating mode to be selected.

Four LEDs indicate when the pause is active, when the buffer unit is empty of data and when the unit is full and the fourth flashes at about 1Hz with a duty cycle proportional to the fullness of the buffer memory.

The software checks the state of the interfaces in turn in a continuous loop. Whenever a data transfer has been acknowledged then the next character is processed. This allows the asynchronous supply of data and retrieval of data from the buffer.

At the end of each loop the status LEDs are updated. A regular timed interrupt is used to initiate a software refresh of the DRAM and test whether the PAUSE switch is pressed or not.

Construction

A soldering iron with a fine tip is needed to prevent solder bridges between the fine tracks of the PCB. Solder all the through pins first.

Unless you are an experienced constructor and have a temperature controlled iron, it is recommended that sockets are

HOW IT WORKS

Whenever a microprocessor has to address more memory than it was originally intended for, there is always the problem of how to split it up. The buffer RAM is divided into 32K blocks — two for the 64K version and eight for the 256K version.

Three of the I/O lines on the 6803 (PI/O-2) act as extra address lines. The main difference between the 64K and 256K DRAM chips is that pin 1 is used for refreshing on the former and address line A8 on the latter. To prevent refresh cycles occuring on the 64K chips during a normal memory access cycle, the two I/O lines which are multiplexed to produce A8 are always kept at logic 1.

The paged DRAM is located between &4000 and &BFFF in the memory map with the EPROM occupying the space from &C000 to &FFFF. The only other memory mapped component, the 6522, is addressed at &100 to &10F in the partially decoded space below &4000. All the 6803's internal RAM, timer, serial and parallel data registers are located in page zero:

&00	Port 1 Data Direction Register
&01	Port 2 Data Direction Register
&02	Port 1 Data Register
&03	Port 2 Data Register
&04–07	Unused, External Memory
&08	Timer Control and Status Register
&09	Counter High Byte
&0A	Counter Low Byte
&0B	Output Compare Register High Byte
&0C	Output Compare Register Low Byte
&0D	Input Capture Register High Byte
&0E	Input Capture Register Low Byte
&0F	Unused, Exernal Memory
&10	Rate and Mode Control Register
&11	Transmit/Receive Control and Status Register
&12	Receive Serial Data Register
&10	Transmit Serial Data Register
&14	RAM Control Register
&15–1F	Reserved
&20–7F	Unused, External Memory
&80–FF	Internal RAM

In order to fit I/O lines onto the 6803 CPU without departing from a 40 pin package, the low order address bus and data bus have been multiplexed. As a consequence each memory access cycle is split in two. During the first half, when the Data Strobe (E) is low, the low order address is placed on the multiplexed bus. The falling edge of the Address Strobe (AS) is provided to latch the data into a transparent latch (IC18).

The non-multiplexed upper address lines and signals such as Read/Write are also stable by this time. The data to be read or written is transferred during the second part of the cycle, when E is high. It is important that the data buffers in peripheral devices are not activated until E is asserted otherwise bus contention will occur.

To keep the DRAM chips as small and cheap as possible, their address lines are multiplexed. Two strobes, Row Address Strobe (RAS) and Column Address Strobe (CAS) are used to latch each half of the address.

The strobes are so named because each DRAM chip has its memory cells arranged as a square matrix of n rows and n columns, where n is 256 for 64K chips and 512 for 256K chips. Strict timings between these signals and the periods of valid data must be adhered to in order to achieve correct operation. See Fig. 3.

The time delay from E rising to RAS falling is different for read and write cycles. During a read cycle, data from the DRAM must be set up in time for it to be accepted by the 6803 and during a write cycle, the DRAM must wait until data from the 6803 is valid before accepting it. The input clock to the 6803, which is divided by four to produce E, is used with a dual D type latch K16 to generate the different RAS/CAS timings. No data has been published by the manufacturers as to the relationship betwen the clock input and the data strobe E. However, tests on several devices show that there is typically a 50ns delay from the falling edge of the clock to a transition of E.

The Read/Write signal is used to modify the time when the IC16 latches are clocked. This is done with an exclusive-OR gate. When reading, the RAS signal is sent low on the first clock transition after E is high — this is the low to high edge. The low half of the address is latched into the DRAM at this point. Two logic gate delays provide the interval between RAS going low and the select signal of the 74LS257 multiplexers changing, so that the other half of the address is ready for when CAS goes low.

On the next clock transition of the same phase, if the correct address is decoded then CAS is sent low. Sufficient time is allowed for the data to be read by the CPU — which latches it on the falling edge of E. RAS and CAS are sent high again when E goes low and thus completes the read cycle.

During the write cycle, the same process as above occurs, but the Read/Write line now makes IC16 clock on the high to low edge of the input clock. This delays the production of RAS and CAS by half a clock period (about 100ns), ensuring the data from the CPU is valid by the time that it is latched into the DRAM by the falling edge of CAS. Since the period of E is fixed, the active part of a DRAM write cycle is 100ns shorter than for a read cycle.

Each time that the DRAM is accessed, all the locations in the column of the row that is addressed are refreshed. To refresh the whole chip, every row must be accessed at intervals of not more than 4ms.

A background program accesses every row once in 4ms. Timed interrupts trigger a program that runs through 256 consecutive bytes of EPROM. By arranging the low order address to be latched by RAS and strobing RAS on every memory access cycle even if the DRAM is not being accessed, the program in EPROM will keep the memory refreshed. A loss of just 5% processing speed results.

Interfaces

The centronics interfaces are connected to a 6522 Versatile Interface Adapator IC20. Port B is used for parallel data output and Port A for parallel data input. Each centronics interface has three handshake lines. When the data has been set up and is stable, the sending unit pulses the STORE line low for a minimum of 0.5μs. The BUSY line is then sent high by the receiving device until it is ready to accept more.

At this point the ACKNOWLEDGE line is given a low pulse by the receiving unit to indicate that the current transfer is complete. The 6522's handshake lines are set to act as STROBE and ACKNOWLEDGE signals for each port although an additional RS flip-flop is required to generate the BUSY signal.

Parallel output data is buffered by a K21 and the handshake lines are buffered using spare gates from IC1. This enables long cables (over 3m) to be used.

The 6803's Serial Communications Interface is programmed to operate in the standard mark/space format with one start bit, one stop bit and no parity. The clock source is derived from the processor clock. A 4.9152MHz crystal must be used to generate the common baud rates of 1200 and 9600.

Consequently, the processor clock is 1.23MHz which requires a 1.25MHz version of the 6803, or better, and a 1.5MHz version of the 6522. It is unlikely a 1MHz 6803 and 6522 will fail to operate under these conditions.

The RTS and CTS handshaking lines are used with no facility for XON/XOFF handshaking. So, a full duplex interface can be split in two, one half to receive data only from the computer and the other to send data only to the printer. This enables serial-serial data transfers to take place concurrently without plug changing. If serial-serial transfers will never be used in a particular application, there is little point in using two D-type connectors.

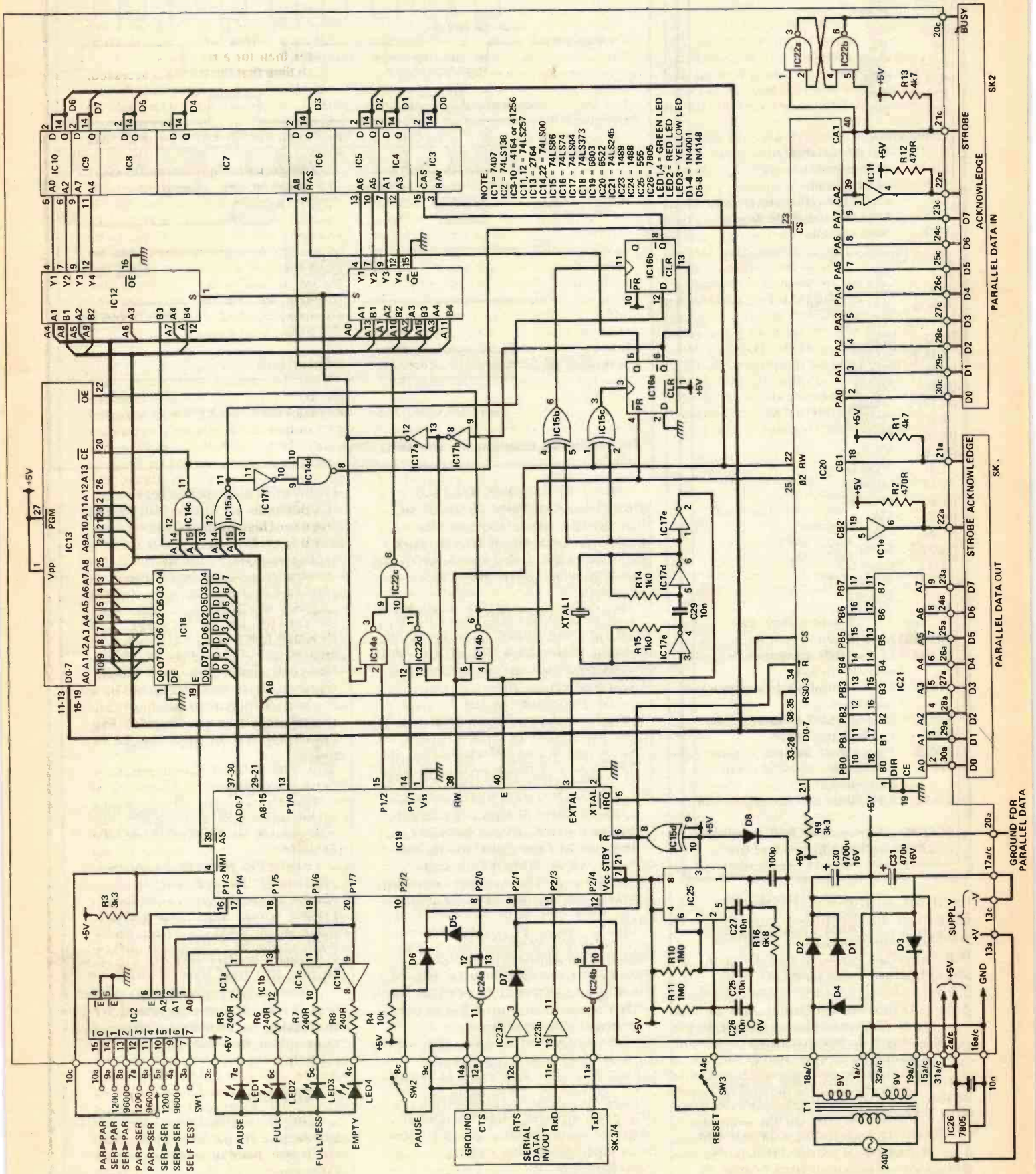


Fig. 2 The circuit diagram of the printer buffer.

PARTS LIST

RESISTORS (all ¼W 5%)

R1,13	4k7
R2,12	470R
R3,9	3k3
R4	10k
R5-8	240R
R10,11	1M0
R14,15	1k0
R16	6k8

CAPACITORS

C1,2	47μ 6V tantalum
C3-28	100n ceramic
C29	10n ceramic
C30	4700μ 16V radial electrolytic
C31	470μ 16V radial electrolytic
C32	100p ceramic

SEMICONDUCTORS

IC1	7407
IC2	75LS138
IC3-10	4164 or 41256
IC11,12	74LS257
IC13	2764
IC14,22	74LS00
IC15	74LS86
IC16	74LS74
IC17	74LS04
IC18	74LS373
IC19	6803
IC20	6522
IC21	74LS245
IC23	MC1489
IC24	MC1488
IC25	555
IC26	7805
LED1,4	Green LED
LED2	Red LED
LED3	Yellow LED
D1-4	1N4001
D5-8	1N4148

MISCELLANEOUS

CON1	64 way DIN 41612 plug & socket
SK1,2	36 way Amphenol Centronics socket
SK3,4	25 way RS232 D socket
SW1	1 pole 8 way rotary
SW2,3	1 pole push button
T1	9-0-9V 30VA toroidal mains transformer
XTAL1	4.9152MHz crystal

PCB; IC sockets; case; PCB standoffs; TO220 mounting kit; nuts and bolts.

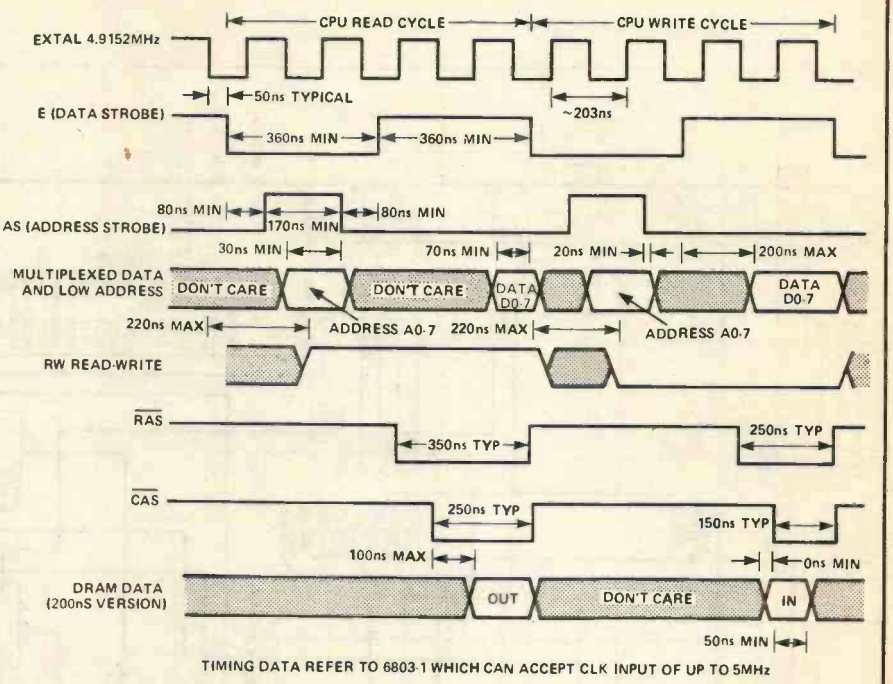


Fig. 3 Timing diagram for the 6803 CPU.

used for all the ICs. However, note that all the holes must be soldered both sides to connect the two PCB foils. In any case a socket should be used for the EPROM (IC13) in case a modified program is ever required.

Figure 5 shows the component overlay for the PCB. Before soldering in the DIN 41612 connector, it should be properly seated on the PCB and then fixed to it with 2.5x10mm bolts.

To ensure that the case of the crystal does not short circuit the tracks on the component side of the board, a piece of insulating material should be fixed to the downward facing side.

The freshly soldered PCB should be carefully cleaned of flux on the underside of the board using a small brush and paraffin, with a finer solvent used afterwards to wash away the paraffin.

Finally, insert the ICs. Avoid wearing man-made clothes so as to keep static to a minimum and always rest ICs on a conducting surface such as the non-painted side of a biscuit tin lid.

Either 4164 or 41256 ICs may be used for IC3-10 to give a buffer size of 64K or 256K. The correct first byte of the EPROM software for the buffer size must be used.

The printer buffer has been designed to fit into a pressed sheet metal box approximately 160mm wide, 80mm tall and 200mm long. The voltage regulator (IC26) bolts to the side of the case.

In the prototype the Centronics connectors are mounted on each side of the box, the RS232 connectors on the back with the switches and LEDs on the front. All connections to off-board components are made via a 64 way DIN 41612 connector located at one end (Fig. 6). Three support locations have been provided on the PCB so that it can be fixed to the base of the box, straddling the mains transformer.

Before drilling any holes, satisfy yourself that the components will all fit together in their intended positions. Remember to allow enough space for the DIN connector to be removed from the PCB with all the wires attached to it.

For greatest safety, the earth of the mains cable should be bolted directly to the base of the case using a spade terminal. If the signal ground potential of any of the units likely to be connected to the buffer is not floating or Earth, then the 7805 regulator must be insulated from the case using standard TO220 insulating washers.

Software

Finally, a programmed EPROM should be plugged into position as IC13.

The EPROM can be either a 2764 or 27128 type and it should be programmed according to Listing 1. For use with a 64K buffer the first byte should contain the number 06. For a 256K buffer the first byte should be 00.

This arrangement also allows a 64K buffer to be upgraded to 256K by replacing the RAM chips and over-programming the first byte with 00.

Testing

Before using the unit a series of checks must be made. Run through the connections to the DIN plug and make sure that all are correct. Take particular care with the supply wires from the transformer. Turn the unit on

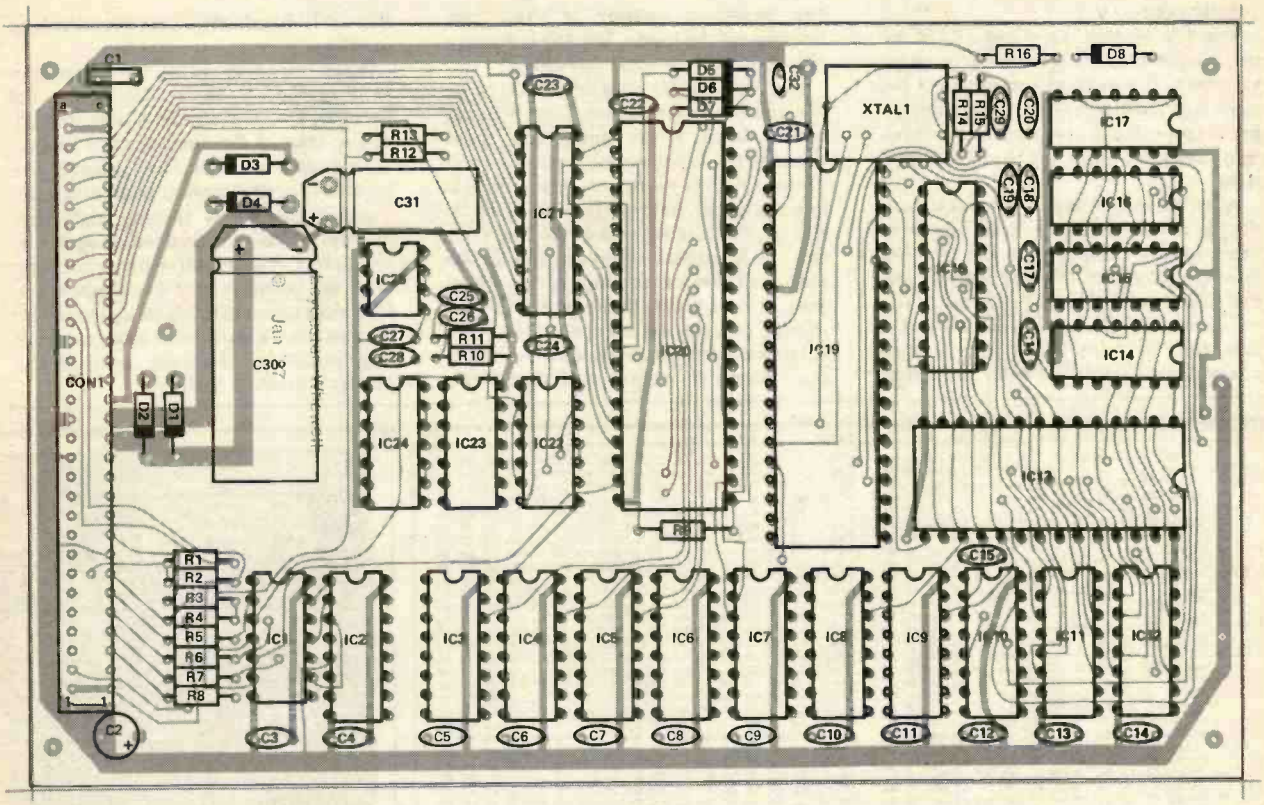


Fig. 4 The component overlay for the printer buffer board.

Pin	Row a	Row b
Pin	Row a	Row b
1	ground	ground
2	+5V	+5V
3	mode 7 select	LED anodes
4	mode 6 select	EMPTY LED cathode
5	mode 5 select	FULLNESS LED cathode
6	mode 4 select	FULL LED cathode
7	mode 3 select	PAUSE LED cathode
8	mode 2 select	PAUSE switch
9	mode 1 select	PAUSE/RESET common
10	mode 0 select	mode select return
11	TxD	RxD
12	CTS	RTS
13	IC24 +V	IC24 –V
14	RS232 ground	RESET switch
15	+V rectified output	+V rectified output
16	7805 regulator ground	7805 regulator ground
17	–V rectified output	–V rectified output
18	T1 secondary I	T1 secondary I
19	T1 secondary II	T1 secondary II
20	Centronics data ground	BUSY (IN)
21	ACKNOWLEDGE (OUT)	ACKNOWLEDGE (IN)
22	STROBE (OUT)	STROBE (IN)
23	D7 (OUT)	D7 (IN)
24	D6 (OUT)	D6 (IN)
25	D5 (OUT)	D5 (IN)
26	D4 (OUT)	D4 (IN)
27	D3 (OUT)	D3 (IN)
28	D2 (OUT)	D2 (IN)
29	D1 (OUT)	D1 (IN)
30	DO (OUT)	DO (IN)
31	+5V	+5V
32	transformer ground	transformer ground

Table 1 DIN 41612 connector pin-out.

Pin	Function
1	Strobe
2	D0
3	D1
4	D2
5	D3
6	D4
7	D5
8	D6
9	D7
10	Acknowledge
11	Busy
12-18	Not connected
19-28	Ground
29-36	Not connected

Table 2 Centronics interface connections.

Pin	Function
2	TxD
3	RxD
4	RTS
5	CTS
7	Ground

Table 3 RS232 interface connections.

Software

The 128 bytes of zero page RAM are used both for the stack and program variables. The main requirement of the stack is to store registers during a refresh interrupt — using seven bytes at a time. This leaves the entire DRAM free to hold data.

After the buffer has been reset it must decide which operating mode it is in. In order to save components, the CPU I/O lines connected to the LED outputs also drive the mode select decoder (IC2). The decoder is enabled and each output is selected in turn until the return connection causes an NMI interrupt. The selected output at that time determines the mode. The I/O lines then revert to their normal operation.

The main buffer program selected by the mode switch consists of a never ending loop. If the buffer has spare capacity, the input source is checked and if more data is ready it is read and put into the buffer. In the case of serial input, if there are less than 64 bytes free then the CTS handshake line is negated. The loop then checks the status of the output port. If there is data in the buffer and the printer is ready to accept it (either by acknowledging the previous byte sent to the Centronics output or asserting the RTS serial handshake line) the next byte is sent.

Again, for serial inputs, the CTS output is asserted if there are over 128 bytes free in the buffer. A branch back to the start of the loop is then made.

This alternate sampling ensures the printer is kept supplied with data even if the computer is sending data very rapidly. When receiving serial input, any characters that result from a framing error are ignored. It is less annoying to find a character missing in a pice of text than to have a corrupted character ruin a printout by changing one of the printer's internal settings.

```
0000    3B 3B 3B 3B 3B 96 02 84 F7 97 02 96 8A 8A 80
0010 97 8A 3B 86 FF 4C 81 08 27 13 97 8A 16 58 58 58
0020 58 58 CA 08 D7 02 01 01 7D 00 8A 2A E8 96 8A 84
0030 07 97 8A 39 86 FF B7 01 02 4F B7 01 00 B7 01 03
0040 86 41 B7 01 08 86 AC B7 01 0C 86 AA B7 01 0C 7F
0050 01 04 86 09 B7 01 05 86 FF B7 01 0D 86 C0 B7 01
0060 0E 7F 00 89 39 0F BE 00 FF BD E0 34 86 FF 97 00
0070 86 76 97 02 86 01 97 01 97 03 B6 E0 00 97 82 97
0080 83 97 86 CE 40 00 DF 84 DF 87 7F 00 8B 7F 00 8C
0090 7F 00 BD 7F 00 8E 7F 00 8F 0E BD E0 13 86 76 97
00A0 02 D6 8A 26 03 7E E1 F8 C1 07 27 19 5A 86 06 54
00B0 24 02 86 05 97 10 5B CE E0 BF 3A EE 00 6E 00 E2
00C0 A7 E3 96 E4 56 BD E0 E8 26 06 96 02 88 B0 97 02
00D0 BD E1 83 26 06 96 02 88 40 97 02 BD E1 CC 26 E5
00E0 96 02 88 20 97 02 20 DD BD E0 F4 CE 06 DB 09 26
00F0 FD 7E E1 33 D6 02 C4 F0 DA 82 D7 02 86 EA C6 08
0100 CE 40 00 4C A7 00 8B 2D A7 01 8B 2D A7 02 8B 2D
0110 A7 03 8B 2D A7 04 8B 2D A7 05 8B 2D A7 06 8B 2D
0120 A7 07 8B 2D 3A BC C0 00 26 D9 4C 7C 00 02 D5 02
0130 27 CE 39 D6 02 C4 F0 DA B2 D7 02 86 EA C6 08 CE
0140 40 00 4C A1 00 26 3B 8B 2D A1 01 26 35 8B 2D A1
0150 02 26 2F 8B 2D A1 03 26 29 8B 2D A1 04 26 23 8B
0160 2D A1 05 26 1D 8B 2D A1 06 26 17 8B 2D A1 07 26
0170 11 8B 2D 3A BC C0 00 26 C9 4C 7C 00 02 D5 02 27
0180 BE 4F 39 C6 06 BD 04 26 F9 C6 05 D7 10 C6 0A D7
0190 11 96 03 8A 01 97 03 C6 02 D5 03 27 2C 96 03 84
01A0 FE 97 03 D5 03 26 22 7D 00 11 7D 00 12 4F C6 20
01B0 D5 11 27 FC 97 13 D6 11 C4 C0 27 FA C4 40 26 09
01C0 D6 12 11 26 04 4C 26 E6 39 86 FF 39 C6 3F F7 01
01D0 0E B7 01 0D 4F B7 01 00 01 01 C6 02 F5 01 0D 27
01E0 14 F6 01 01 11 26 0E C6 10 F5 01 0D 27 07 F7 01
01F0 0D 4C 26 E1 39 C6 FF 39 86 02 B5 01 0D 27 FB B6
0200 01 01 B7 01 00 D6 86 DE B7 0B 8C C0 00 26 0A CE
0210 40 00 5C C1 0B 26 02 D6 B2 9C B4 26 0C D1 83 26
0220 0B 96 02 84 DF 97 02 20 32 B6 01 0D B4 02 27 2B
0230 B6 01 01 D6 02 C4 FB DA B6 D7 02 DE B7 A7 00 D6
0240 B6 0B 8C C0 00 26 0A CE 40 00 5C C1 0B 26 02 D6
0250 B2 DF B7 D7 B6 96 02 BA B0 97 02 B6 01 0D B4 10
0260 27 A3 D6 B3 DE B4 9C B7 26 0C D1 B6 26 0B 96 02
0270 B4 7F 97 02 20 B3 7D 00 BF 2B BA D6 02 C4 FB DA
0280 B3 D7 02 A6 00 B7 01 00 D6 B3 0B 8C C0 00 26 0A
0290 CE 40 00 5C C1 0B 26 02 D6 B2 DF B4 D7 B3 96 02
02A0 BA 20 97 02 7E E2 05 B6 0B 97 11 96 03 B4 FE 97
02B0 03 96 11 84 C0 27 FA 2B 04 96 12 20 F4 96 12 B7
02C0 01 00 DC B7 C3 00 40 37 D6 B6 B1 C0 26 09 B0 B0
02D0 5C C1 0B 26 02 D6 B2 36 3B 9C B4 26 12 D1 B3 26
02E0 0E 96 02 84 DF 97 02 96 03 BA 01 97 03 20 36 96
02F0 11 B4 C0 27 30 2B 04 96 12 20 2A 96 12 D6 02 C4
0300 FB DA B6 D7 02 DE B7 A7 00 D6 B6 0B 8C C0 00 26
0310 0A CE 40 00 5C C1 0B 26 02 D6 B2 DF B7 D7 B6 96
0320 02 BA B0 97 02 B6 01 0D B4 10 27 96 D6 B3 DE B4
0330 9C B7 26 0C D1 B6 26 0B 96 02 B4 7F 97 02 20 AF
0340 7D 00 BF 2B 4E D6 02 C4 FB DA B3 D7 02 A6 00 B7
0350 01 00 D6 B3 0B 8C C0 00 26 0A CE 40 00 5C C1 0B
0360 26 02 D6 B2 DF B4 D7 B3 96 02 BA 20 97 02 DC B7
0370 C3 00 B0 37 D6 B6 B1 C0 26 09 B0 B0 5C C1 0B 26
0380 02 D6 B2 36 3B 9C B4 26 0A D1 B3 26 06 96 03 B4
0390 FE 97 03 7E E2 C2 B6 02 97 11 B5 01 0D 27 FB B6
03A0 20 95 11 27 FC B6 02 95 03 26 FC B6 01 01 97 13
03B0 D6 B6 DE B7 0B 8C C0 00 26 0A CE 40 00 5C C1 0B
03C0 26 02 D6 B2 9C B4 26 0C D1 B3 26 0B 96 02 B4 DF
03D0 97 02 20 32 B6 01 0D B4 02 27 2B B6 01 01 D6 02
03E0 C4 F8 DA B6 D7 02 DE B7 A7 00 D6 B6 0B 8C C0 00
03F0 26 0A CE 40 00 5C C1 0B 26 02 D6 B2 DF B7 D7 B6
0400 96 02 8A B0 97 02 B6 02 95 03 26 A4 B6 20 95 11
0410 27 9E D6 B3 DE B4 9C B7 26 0C D1 B6 26 0B 96 02
0420 B4 7F 97 02 20 AE 7D 00 BF 2B B5 D6 02 C4 F8 DA
0430 B3 D7 02 A6 00 97 13 D6 B3 0B 8C C0 00 26 0A CE
0440 40 00 5C C1 0B 26 02 D6 B2 DF B4 D7 B3 96 02 8A
0450 20 97 02 7E E3 B0 B6 0A 97 11 96 03 B4 FE 97 03
0460 DC B7 C3 00 40 37 D6 B6 B1 C0 26 09 B0 B0 5C C1
0470 0B 26 02 D6 B2 36 3B 9C B4 26 12 D1 B3 26 0E 96
0480 02 B4 DF 97 02 96 03 BA 01 97 03 20 36 96 11 B4
0490 C0 27 FA 2B 04 96 12 20 2A 96 12 D6 02 C4 F8 DA
04A0 B6 D7 02 DE B7 A7 00 D6 B6 0B 8C C0 00 26 0A CE
04B0 40 00 5C C1 0B 26 02 D6 B2 DF B7 D7 B6 96 02 8A
04C0 B0 97 02 B6 02 95 03 26 97 B6 20 95 11 27 91 D6
04D0 B3 DE B4 9C B7 26 0C D1 B6 26 0B 96 02 B4 7F 97
04E0 02 20 AA 7D 00 BF 2B 4D D6 02 C4 F8 DA B3 D7 02
04F0 A6 00 97 13 D6 B3 0B 8C C0 00 26 0A CE 40 00 5C
0500 C1 0B 26 02 D6 B2 DF B4 D7 B3 96 02 BA 20 97 02
0510 DC B7 C3 00 B0 37 D6 B6 B1 C0 26 09 B0 B0 5C C1
0520 0B 26 02 D6 B2 36 3B 9C B4 26 0A D1 B3 26 06 96
0530 03 B4 FE 97 03 7E E4 60 B6 01 0D B4 01 0E B5 40
0540 27 45 C6 40 F7 01 0D 8D 70 8D 3D 96 8A B1 07 27
0550 36 DE 8B 9C 8D 26 06 D6 02 CA 40 D7 02 0B DF 8B
0560 8C 02 00 26 22 7F 00 8B DC B7 93 84 16 07 58 06
0570 96 86 92 83 7D E0 00 26 02 04 04 84 01 DD 8D 27
0580 06 96 02 84 BF 97 02 3B B6 04 95 03 26 24 B6 0B
0590 95 8F 26 1D 7C 00 BF 95 8F 27 16 D6 BF 17 C4 80
05A0 54 54 54 D7 90 8B 80 97 BF D6 02 C4 EF DA 90 D7
05B0 02 39 96 BF B4 80 97 BF 39 73 00 89 2B 7F CE 00
05C0 00 CE 00 01 CE 00 02 CE 00 03 CE 00 04 CE 00 05
05D0 CE 00 06 CE 00 07 CE 00 08 CE 00 09 CE 00 0A CE
05E0 00 0B CE 00 0C CE 00 0D CE 00 0E CE 00 0F CE 00
05F0 10 CE 00 11 CE 00 12 CE 00 13 CE 00 14 CE 00 15
0600 CE 00 16 CE 00 17 CE 00 18 CE 00 19 CE 00 1A CE
0610 00 1B CE 00 1C CE 00 1D CE 00 1E CE 00 1F CE 00
0620 20 CE 00 21 CE 00 22 CE 00 23 CE 00 24 CE 00 25
0630 CE 00 26 CE 00 27 CE 00 28 CE 00 29 39 CE 00 00
0640 CE 00 01 CE 00 02 CE 00 03 CE 00 04 CE 00 05 CE
0650 00 06 CE 00 07 CE 00 08 CE 00 09 CE 00 0A CE 00
0660 08 CE 00 0C CE 00 0D CE 00 0E CE 00 0F CE 00 10
0670 CE 00 11 CE 00 12 CE 00 13 CE 00 14 CE 00 15 CE
0680 00 16 CE 00 17 CE 00 18 CE 00 19 CE 00 1A CE 00
0690 1B CE 00 1C CE 00 1D CE 00 1E CE 00 1F CE 00 20
06A0 CE 00 21 CE 00 22 CE 00 23 CE 00 24 CE 00 25 CE
06B0 00 26 CE 00 27 CE 00 28 39 00 00 00 00 00 00 00
1F00 2A 2A 2A 2A 2A 2A 2A 2A 2A 2A 2A 2A 2A 2A 2A 2A
1F10 50 72 69 6E 74 65 72 20 42 75 66 66 65 72 20 20
1F20 68 61 72 64 77 61 72 65 2C 20 20 20 20 20 20 20
1F30 73 6F 66 74 77 61 72 65 20 61 6E 64 20 20 20 20
1F40 50 43 42 20 64 65 73 69 67 6E 20 62 79 20 20 20
1F50 4C 65 79 63 65 73 74 65 72 20 20 20 20 20 20 20
1F60 57 68 65 77 65 6C 20 20 20 20 20 20 20 20 20 20
1F70 33 72 64 20 4D 61 72 63 68 20 31 39 38 37 20 20
1F80 2A 2A 2A 2A 2A 2A 2A 2A 2A 2A 2A 2A 2A 2A 2A 2A
1FF0 E0 01 E0 02 E0 03 E0 04 E5 38 E0 05 E0 06 E0 65
```

Listing 1 Hex dump of the used sections of the EPROM (see text for first byte).

BUYLINES

The printer buffer uses components which are for the most part easily obtainable from usual suppliers. The case used for the prototype is available from Maplin (part no. XB71N). The 6803 can be bought from Midwich (Tel: (0379) 4131).

The PCB is available from the ETI PCB Service see the back of this issue for details.

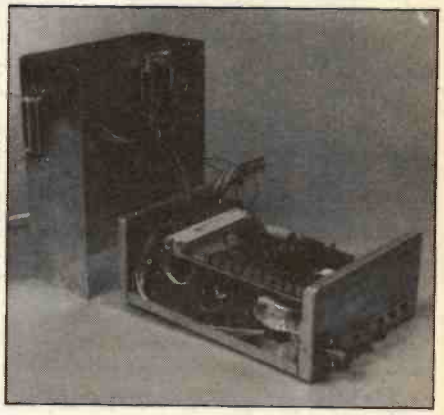
The author can supply the source code (£7.50) or the source code and a 6803 assembler (£15) copied onto formatted BBC micro disks supplied by readers.

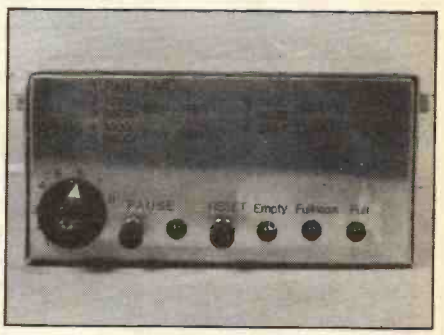
Programmed EPROMs are available for £6 (reader's 2764 or 27128 EPROM) or £9 (EPROM supplied). Please specify whether the 64K or 256K version is required.

The author will also build and test boards purchased from the PCB service for £70. This includes all on-board components but not the case, switches, connectors and so forth. Please address all enquiries and orders to Leycester Whewell, St. Just, Berrington Road, Tenbury Wells, WR15 8EJ.

without the PCB plugged in and check that each of the supply inputs read 9V relative to ground and that they are at 18V relative to each other.

Plug in the PCB and run the unit in the self test mode. The memory test involves writing to every byte of RAM, waiting 10ms to check the refresh system and

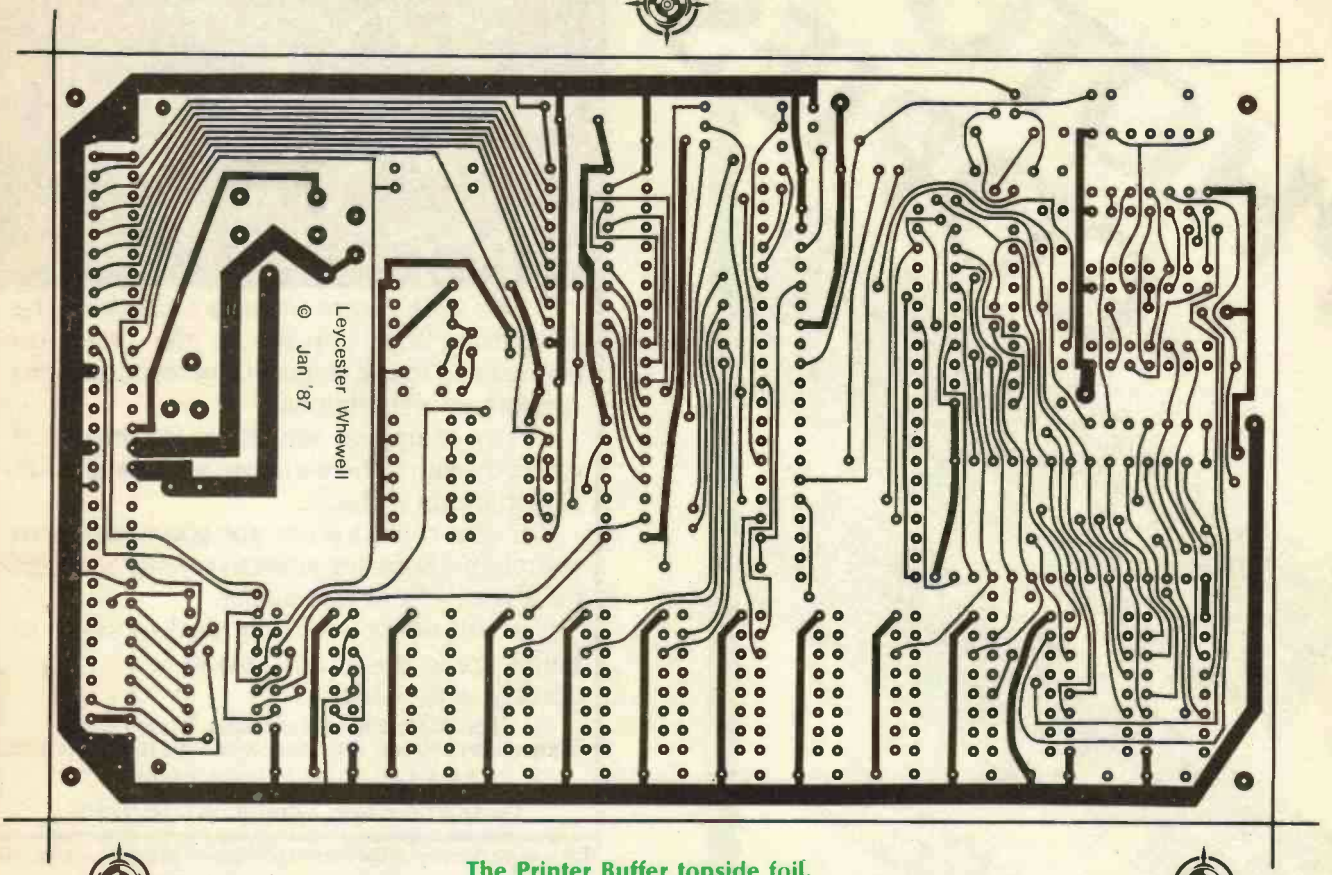




then verifying that data. If successful, the EMPTY LED is toggled and next time the process is repeated with a different arrangement of data. A full check on 256K of RAM takes a couple of seconds.

To check the parallel ports, a lead with a Centronics connector at each end is required. By connecting the output to the input, a check is made on the transfer of 256 bytes of data. When the data is verified and separate tests on the handshake lines are satisfactory then the FULL LED is toggled.

The serial interface is checked in a similar way — by connecting the data lines and the handshake lines together. Tests are performed at 1200 and 9600 baud and if successful, the FULLNESS LED is toggled. If all is well, the buffer is now ready to earn its keep. **ETI**



The Printer Buffer topside foil.

The Printer Buffer solderside foil.